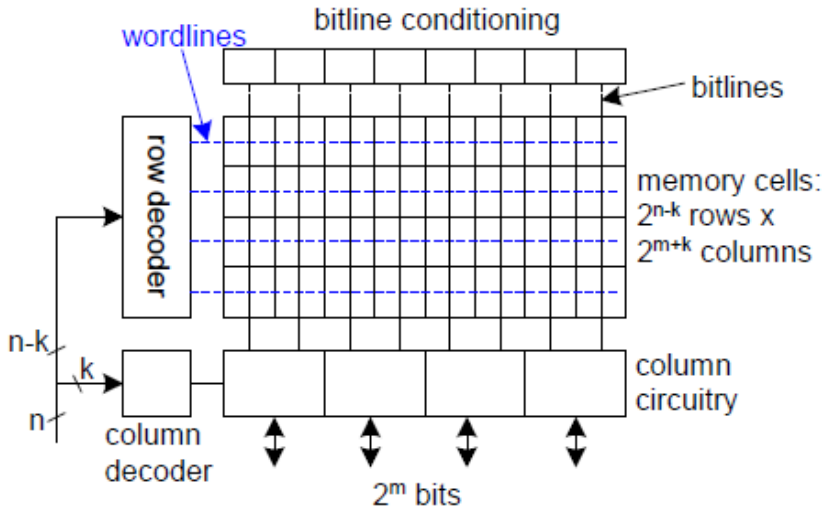
Name:_____

Session 5: Full memory array

The objective of this session is to create a full memory array with its decoders, multiplexers and sense amplifiers.

Memory block

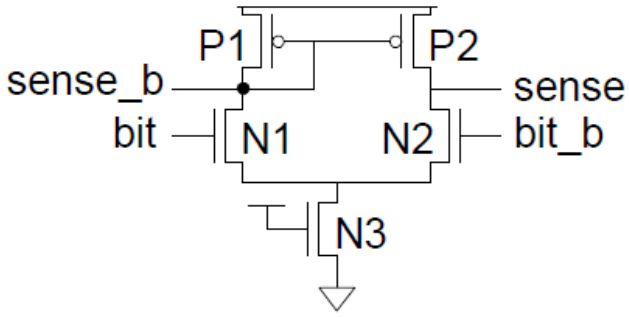
The following picture depicts one memory array;

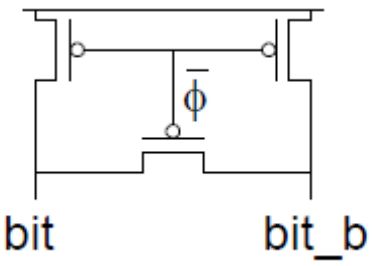


In the previous labs, we have worked on the memory cells. Now we need to add all the peripheral circuitry.

1. Bitline conditioning and column circuitry

Implement the following sense amplifier (figure on the left) or any alternative presented in class. Attach it to all the columns.





Bitlines need to be precharged before they can be used. Use the above circuitry on the right for each column.

Apart from that we will need the row decoder. Look into the course slides for decoder examples. Build one into your memory array to activate the corresponding wordline (given a memory address).

2. Memory array timing

Memory operations require a careful timing of the block. The designer must set specific timing requirements to activate the precharge signal (Φ) and the sense amplifier signal (if needed). Thus, we will have to implement the timing logic.
This is done through an original clock signal as a baseline. This baseline signal is then delayed (through a series of inverters) so that the delay introduced by these inverters defines the timing of that specific signal.

First, measure the timing requirements of your memory:
1. Precharge time (precharge the bitlines)
2. Access time (from the initial memory address, activate the right wordline, write or read the cell contents and go through the senseamplifiers)
3. Memory array total access time (i.e. at what clock rate it can operate)

Once these timings are set, build up a circuit that effectively activates the appropriate signals at the right time.

Questions:

1. What is the timing of your memory?

Measure of the delay		
Scenario (rows/columns)	**Precharge time**	**Access time**
64/64		
64/128		
64/256		
128/64		
128/128		
128/256		
256/64		
256/128		
256/256		

2. Measure the read and write times for different number of columns and rows.

Measure of the delay		
Scenario (rows/columns)	**Read**	**Write**
64/64		
64/128		
64/256		
128/64		
128/128		
128/256		
256/64		
256/128		
256/256		

Lab session 5 review form		
How long did it take you to complete the lab?		
Is the documentation clear?	YES	NO
What can be improved?		