Name:____

Session 4: Variability Injection

The objective of this session is to evaluate the performance of different SRAM cell designs in the presence of process variations.

Process variations

Imperfections in the manufacturing process lead to undeterministic cell layouts and material compositions. At the same time, dynamic conditions (such as temperature) impact also the characteristics of the device and, eventually, it may change its performance.
The following table[1] summarizes the most common sources of mismatch:

Proximity	Spatial	Temporal	
		Reversible	Irreversible
Inter Die Variation	Parameter (L_G,V_T,t_{ox}) T V_{th} L_{eff}	Environmental Operating Temp T	Hot-Electron Effect T
		Activity Factor T	NBTI shift V_{th}
Intra Die Variation	Pattern-Density/Layout Induced L_{eff}	On-Die Hot Spots T	Hot Spot Enhanced NBTI V_{th}
Device-to-Device Variation	Atomistic Dopant Variation V_{th}	SOI Body History Self Heating T	$Dev_{VT-NBTI}$ (NBTI induced V_T Distribution) V_{th} T
	Line-edge Roughness L_{eff}		
	Parameter Std.dev V_{th} L_{eff}		

Parameters Affected
T - Temperature
V_{th} - Threshold
L_{eff} - Effective Length

These different effects have different weights in the final variation characterization and they can even compensate each other as there is no relation among them. There are two big classes of variation: spatial (usually referred as process variations) and temporal (depending on the amount of time spent in stress conditions). In class, we will get in this matter in more detail. At this point, we just need to know that all these effects can be simulated as a shift in the Vth. Thus, in this lab we will focus only on this parameter.
In terms of simulation, as the different sources of variation are uncorrelated, it becomes a statistical matter to simulate a sufficiently large number of samples and then obtain the performance distribution. This process is statistically known as Montecarlo experiments. This means extracting N random samples of the final distribution of each parameter and running them. If the simulation space is large enough, we will have a characterization of the performance distribution of that circuit under process variations.

[1] Bernstein et al."High Performance CMOS Variability in the 65-nm regime and beyond". IBM JRD, July 2006.

While performing Montecarlo experiments is beyond the scope of this lab session, we will simulate the effect of variability on two circuits: an oscillator ring and a 6T SRAM.

1. Process variations in an oscillator ring

We will first start with an oscillator ring. Connect 4 identical symmetric inverters. Connect a load of 1uF at the end of the 4th inverter (or connect it back to the input of the 1st inverter). In the spice file, measure the propagation delay between the 2nd and 3rd inverter and the delay between the 3rd and the 4th (thus we will get rise and fall times with a single simulation, use the MEASURE command to do this). You can manually change the Vth for each simulation, alternatively, you may use insert a control structure –similar to that to compute the SNM- to run all the sims.

In our model, you can modify the Vth by using the altermod command to change the value of the "tn" or "tp" models. The Vth parameter is called "vth0" in our model. Thus, modify "@tn[vth0]" or "@tp[vth0]" for the following scenarios:

Scenario	Nmos (tn) variation	Pmos (tp) variation
Nominal	0	0
Negative NMOS	-20%	0
Negative PMOS	0	-20%
Negative Both	-20%	-20%
Positive NMOS	20%	0
Positive PMOS	0	20%
Positive Both	20%	20%
Positive NMOS- Negative PMOS	20%	-20%
Negative NMOS- Positive PMOS	-20%	+20%

Question:

1. Measure the rise and fall times for the different scenarios.

Measure of the delay		
Scenario	**Rise**	**Fall**
Nominal		
Negative NMOS		
Negative PMOS		
Negative Both		
Positive NMOS		
Positive PMOS		
Positive Both		
Positive NMOS- Negative PMOS		
Negative NMOS- Positive PMOS		

2. Process variations in a 6T SRAM cell

Given the results in section 1, pick the 2 most negative scenarios and together with the nominal case run simulations for a 6T SRAM cell following the same procedure.

Question:

1. Measure the read 0 and read 1 times for the 2 scenarios.

Measure of the delay		
Scenario	**Read 0**	**Read 1**
Nominal		

Apart from delay, process variations also impact robustness and power consumption. This lab analyzes just the impact on delays.

Lab session 4 review form		
How long did it take you to complete the lab?		
Is the documentation clear?	YES	NO
What can be improved?		