Name:_____

Session 1a: Design and simulation of logic gates with Spice

The objective of this session is to learn how to use the simulator *ngspice* and the viewer *kjwaves*.

Download the two programs to your system. They are cross-platform so you should not have any problem to install them. Follow the links in the course webpage: *http://docencia.ac.upc.edu/master/MIRI/NCD/*

You may configure kjwaves to directly run your ngspice simulations. Just make sure you insert the right path to the ngspice executable in the "Options/Change Simulation Engine" menu.

1. Simulation of two-input NAND gate

Download the following files (model28nm.spi, nand2.spi and run_nand2.spi) into your account.

The file "model28nm.spi" has a description of the type of transistors we will use. These transistors are part of the BSIMv4.0 MOSFET models. This description corresponds to the 28nm node (Thus λ=28nm).

The file "nand2.spi" has a description of the two-input nand gate in the spice language. From this description draw the schematic of the gate (transistors).

The file "run_nand2.spi" has a description of the input values of the circuit when running the simulation.

Let's run the simulation:

```
> ngspice
Spice 1 -> cd [path_to_source_spi_files]
Spice 2 -> source run_nand2.spi
Spice 3 -> run
Spice 4 -> write nand2_out.raw
. . . . .
Spice x -> quit
```

You may generate some plots directly in ngspice. Just insert the following commands after the "run" command:

```
Spice 4 -> display
Spice 5 -> plot signal1 signal2 signal3 ...
```

Alternatively, you may use kjwaves, a more powerful tool to visualize the result of the simulation. Open kjwaves and the "nand2_out.raw" file.

Measure the delay of the output value to change from 0 to 1 and from 1 to 0.

Measure of the delay			
Initial state	**Future state**	**Action**	**Delay (ns)**
Out	**Out'**		
0	1	Raise	
1	0	Fall	

2. Design of a complex gate

Design a gate that implements the function $S = \overline{A + BC}$. Edit a simulation file and run the simulation. Measure the delay of the output.

Gate simulated (schematic)

Measure of the delay			
Initial state	**Future state**	**Action**	**Delay (ns)**
Out	**Out'**		
0	1	Raise	
1	0	Fall	

How to measure delays in Spice

All through this course, we will always measure the delay as the elapsed time from the moment the input signal has changed a 20% of its value until the output signal has changed 80% of its value

Session 1b: Design of a CMOS inverter

The objective of this session is to see the effect of the design parameters (L and W) of an inverter over delay and the transfer function.

1. Design of a minimum size inverter

The session starts with the smallest inverter that can be build (L=2λ, W=2λ). Design the inverter, connect consecutively two of them and make the following simulations:

1. Simulate the pair of inverters with an input signal that oscillates taking 0'5ns to move from 0 to 1 and from 1 to 0 (slope). Measure the charge and discharge time of the output of the first transistor.
2. Simulate the pair of inverters with an input signal that changes slowly from 0 to 1 (e.g. 15s). Visualize the input signal against the output of the first inverter (transfer function)

Questions:

1. Discharge time (ns):
2. Charge time(ns):
3. How does the transfer function look like? Is it symmetrical? Is it shifted to the left or to the right?

Measure of the delay			
Output Value		**Action**	**Delay (ns)**
Initial	**Final**		
		Raise	
		Fall	

Transfer function			
Is the transfer function symmetrical?	YES	NO	
Is it shifted to the left or to the right?	Right	Left	Don't know

2. Design of a symmetric inverter

Re-design the inverter to make it as symmetrical as possible. Repeat the same simulations as before.

Questions:

1. Discharge time (ns):
2. Charge time (ns):
3. How does the transfer function look like? In what voltage is it centered?
4. What modifications have you introduced to the original inverter?

Measure of the delay			
Initial state	**Future state**	**Action**	**Delay (ns)**
Out	**Out'**		
		Raise	
		Fall	
Transfer function			
In what voltage is it centered?			
What modifications have you introduced to the original inverter?			