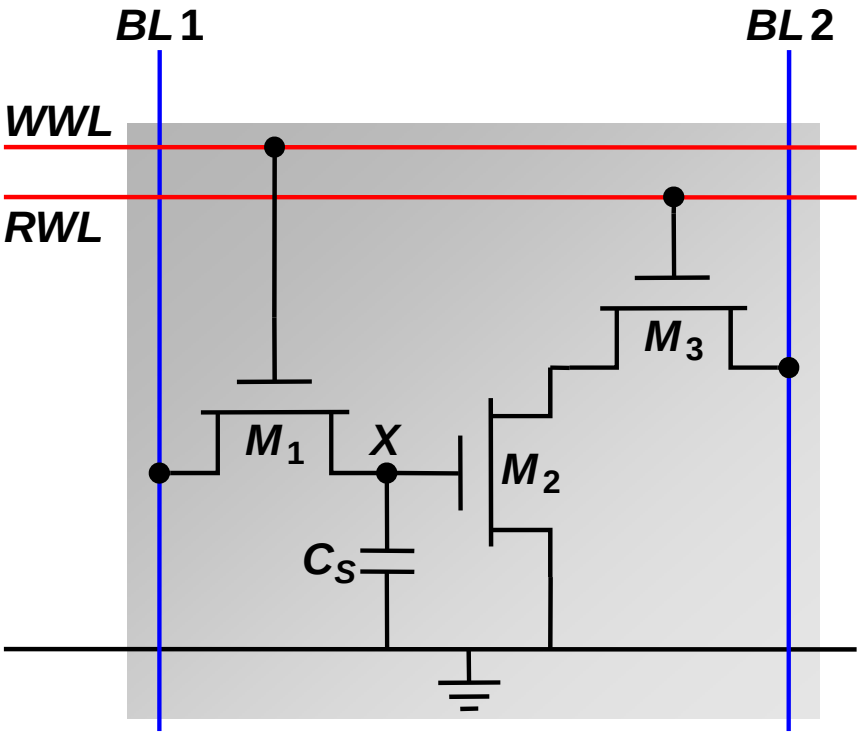
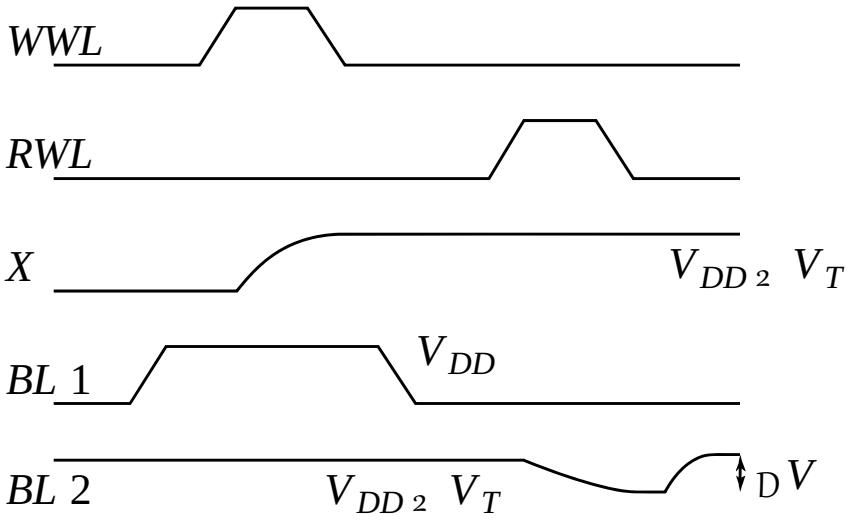
Memory Structures: DRAM cells

Ramon Canal
NCD - Master MIRI

3-Transistor DRAM Cell



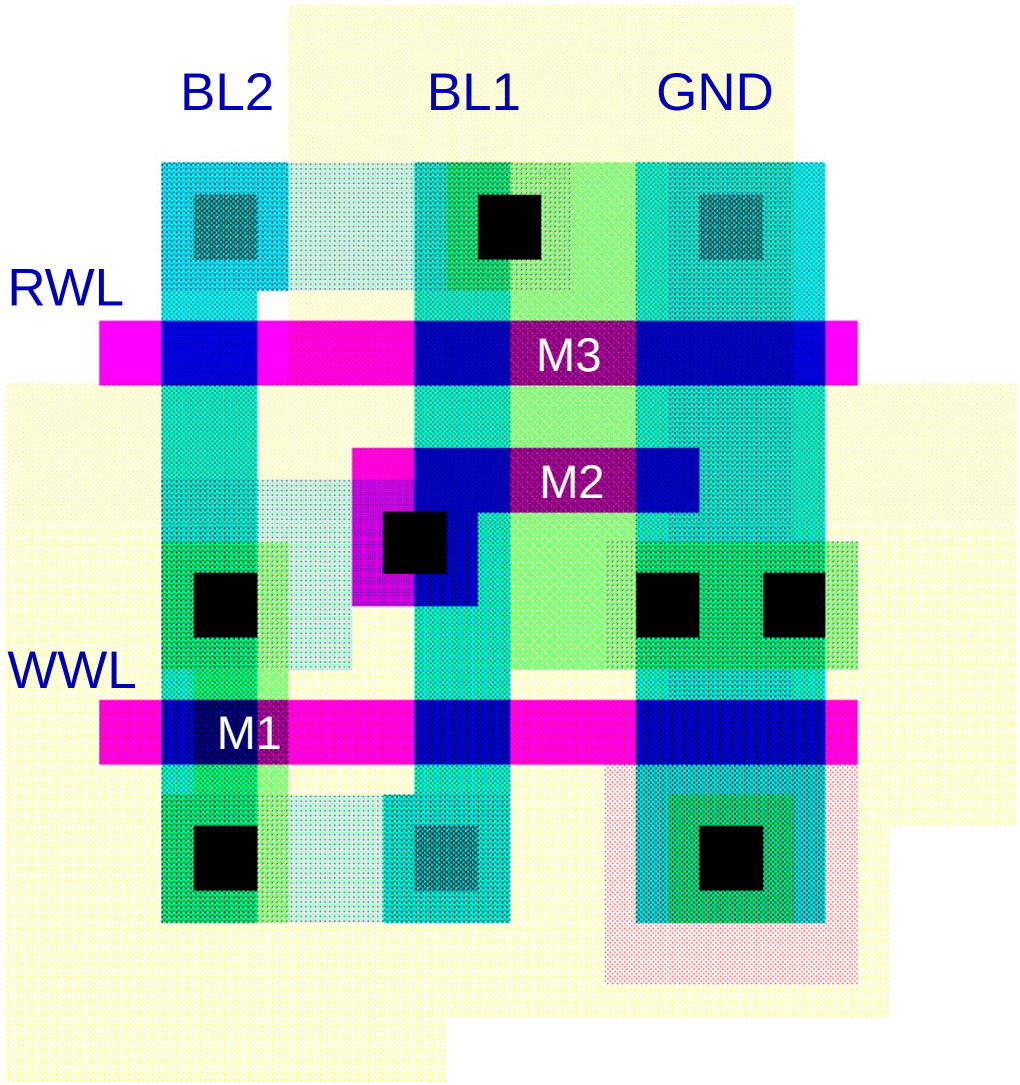


No constraints on device ratios

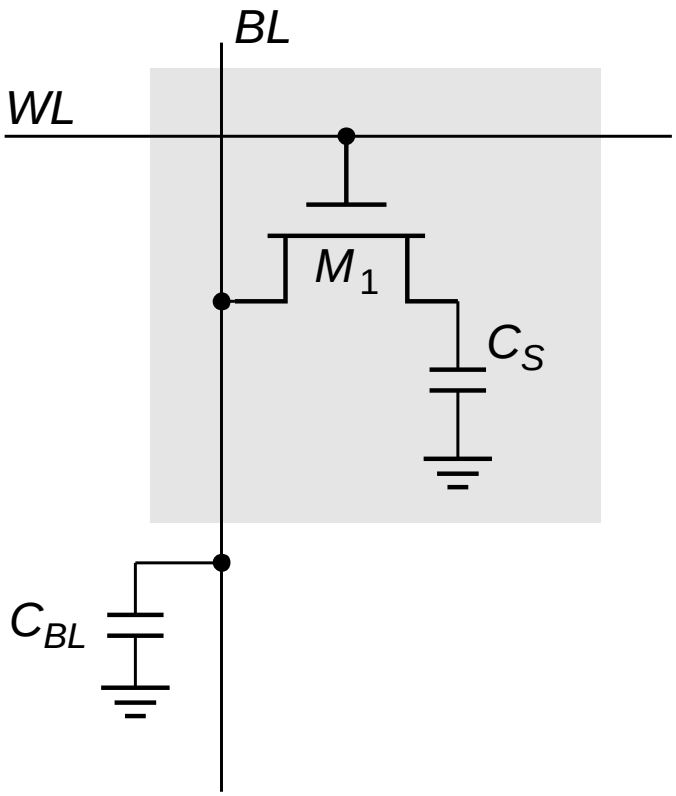
Reads are non-destructive

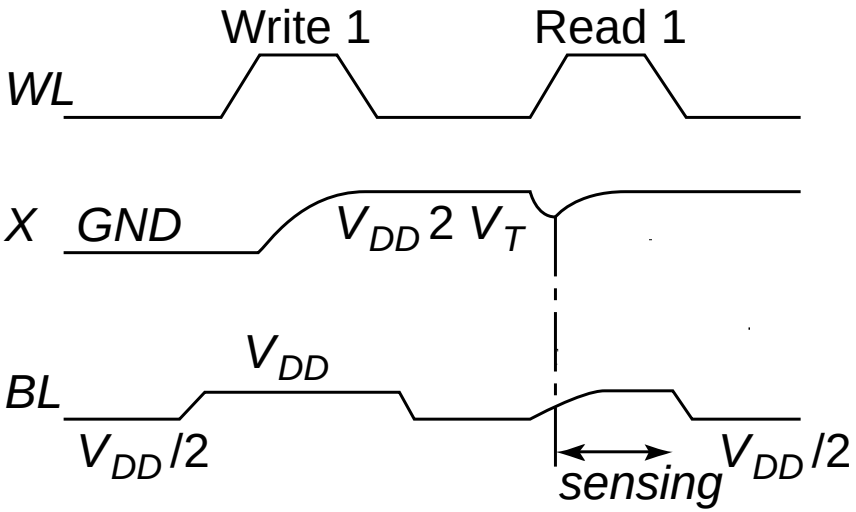
Value stored at node X when writing a "1" = V^{WWL}-V^{Tn}

3T-DRAM — Layout



1-Transistor DRAM Cell





Write: C_S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes places between bit line and storage capacitance

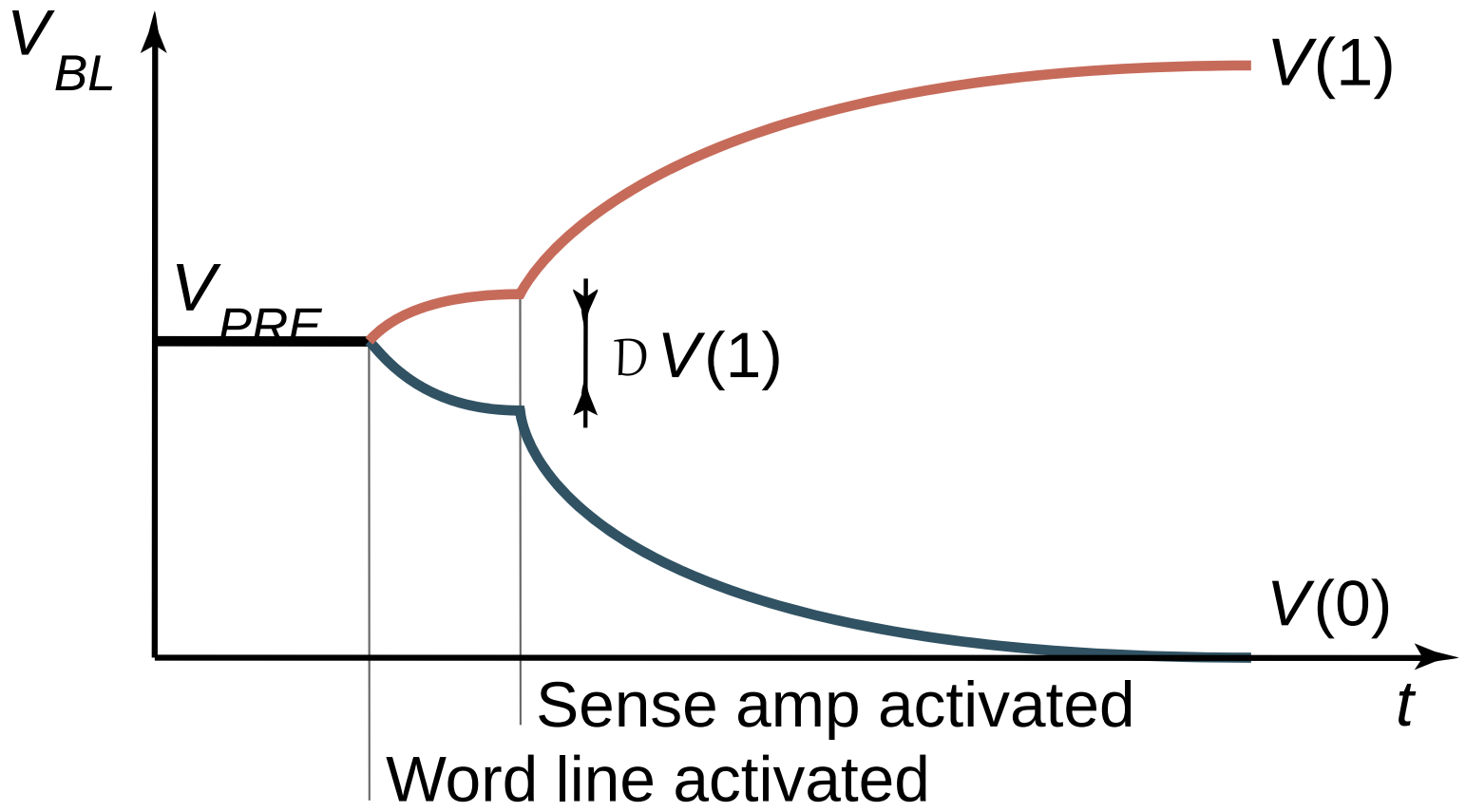
$$\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

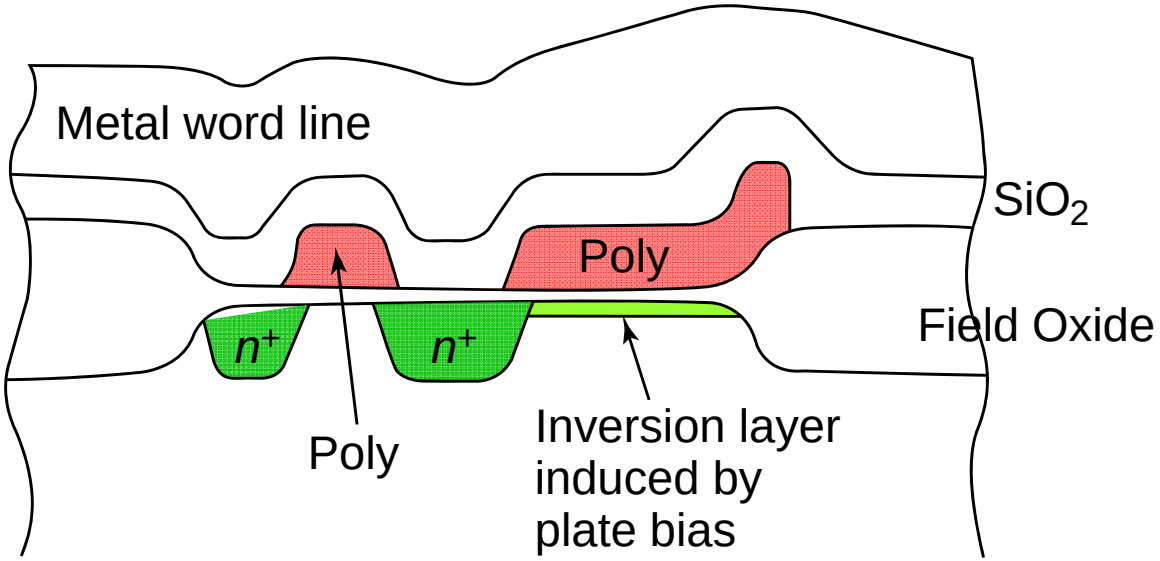
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}

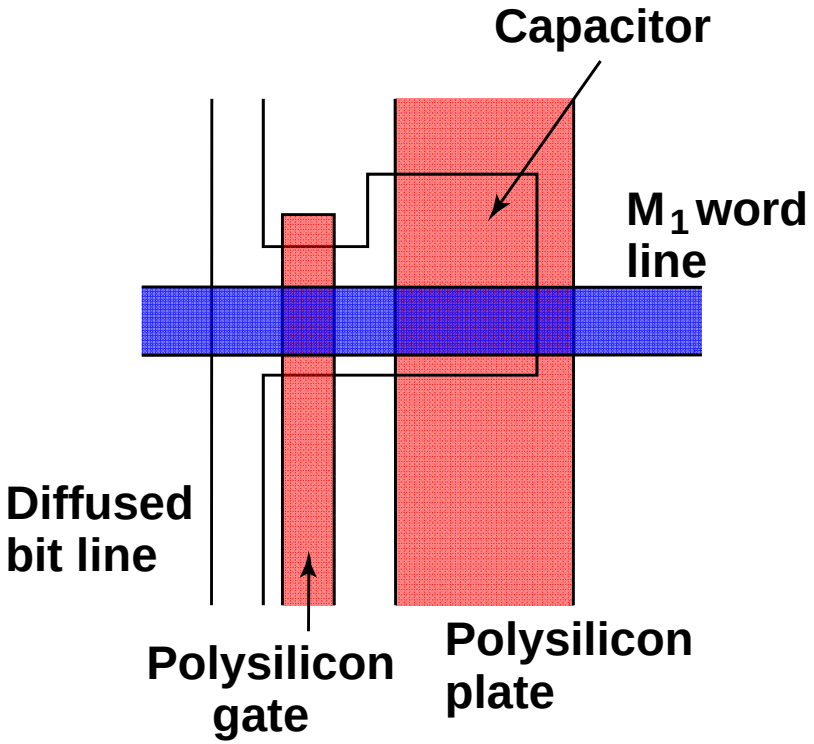
Sense Amp Operation



1-T DRAM Cell



Cross-section

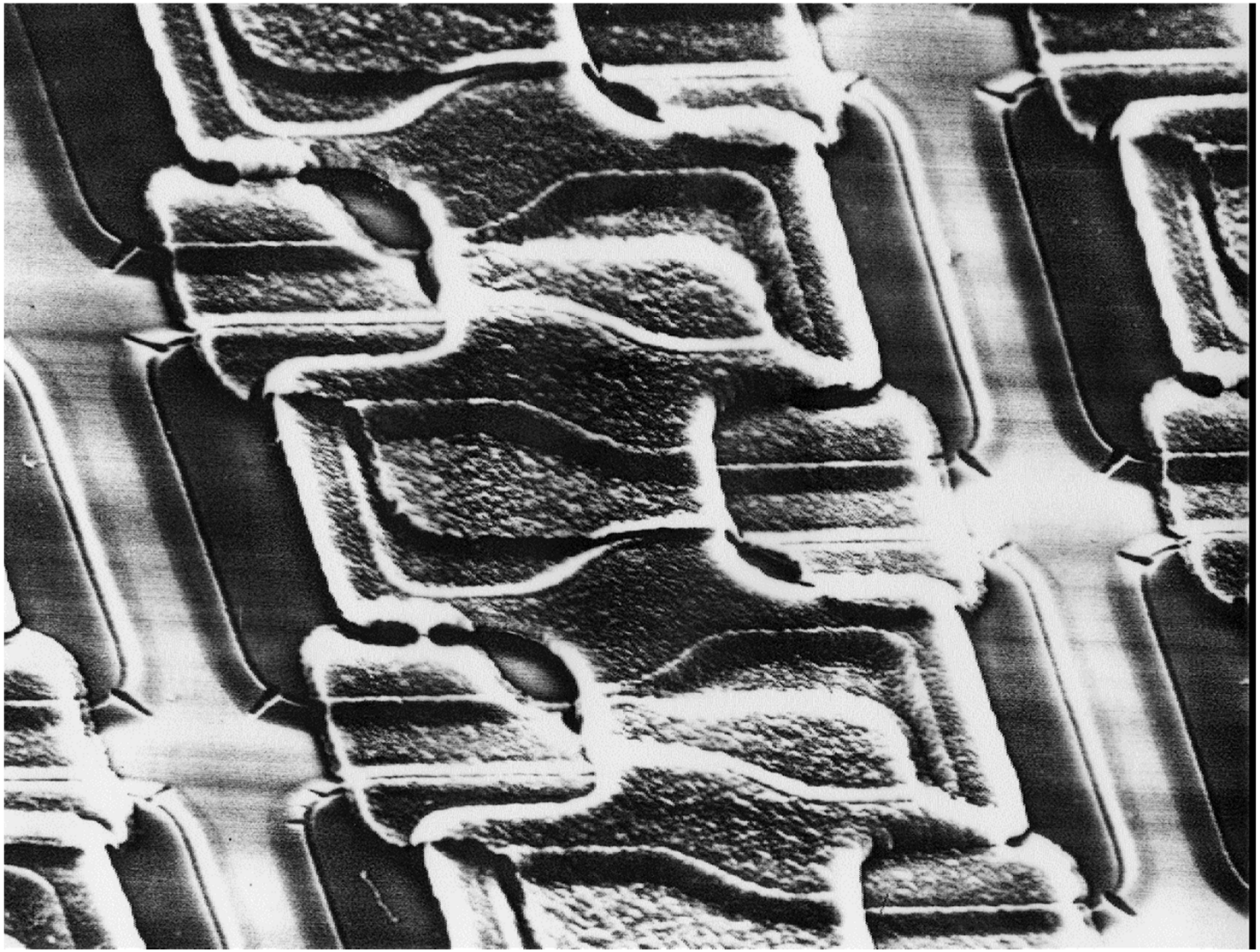


Layout

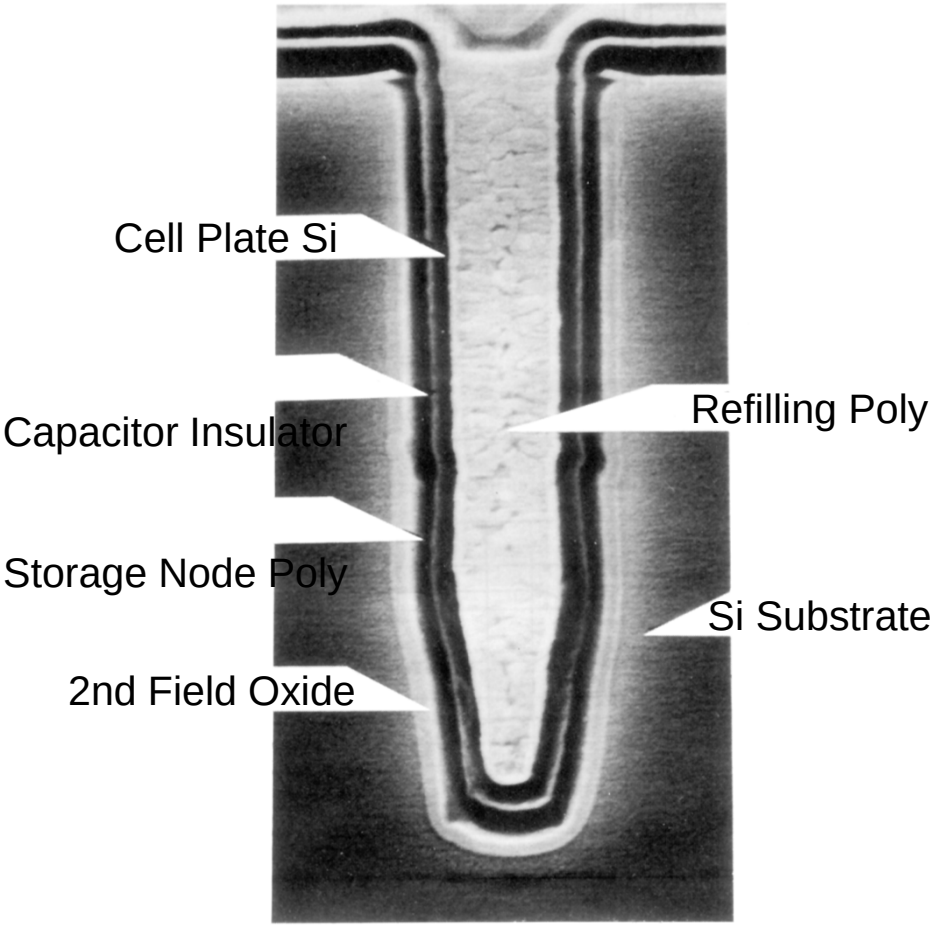
Uses Polysilicon-Diffusion Capacitance

Expensive in Area

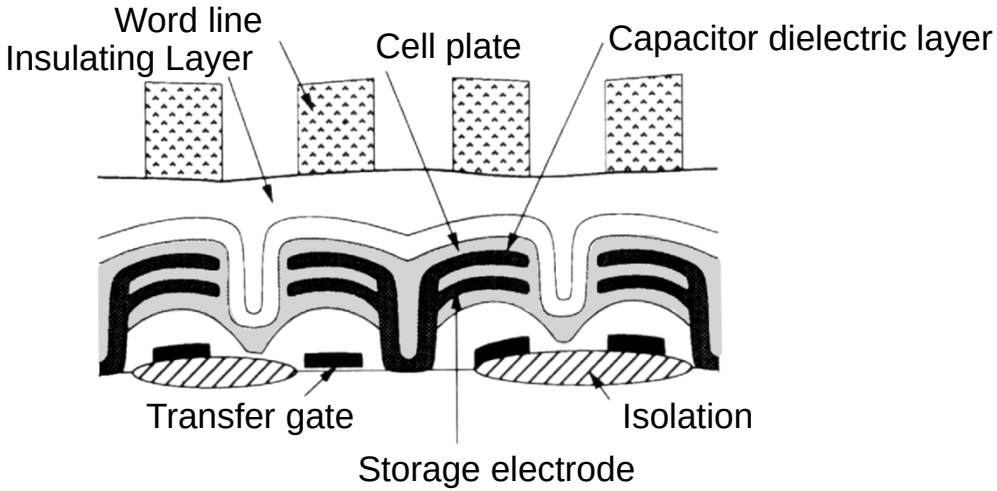
SEM of poly-diffusion capacitor 1T-DRAM

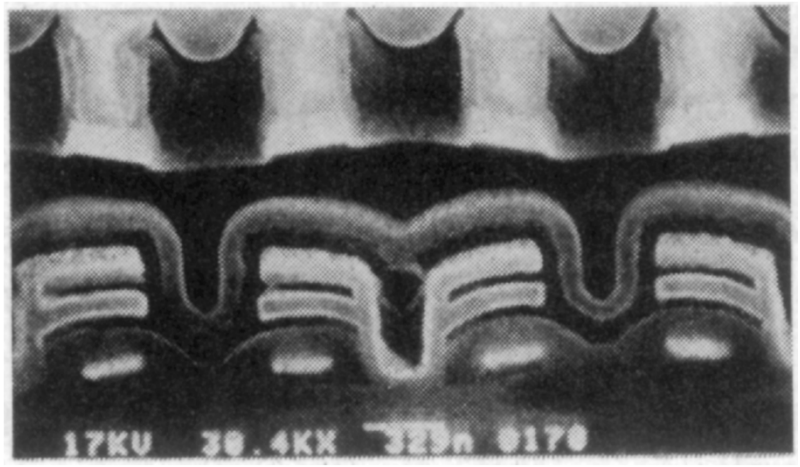


Advanced 1T DRAM Cells



Trench Cell





Stacked-capacitor Cell

Novel cell designs

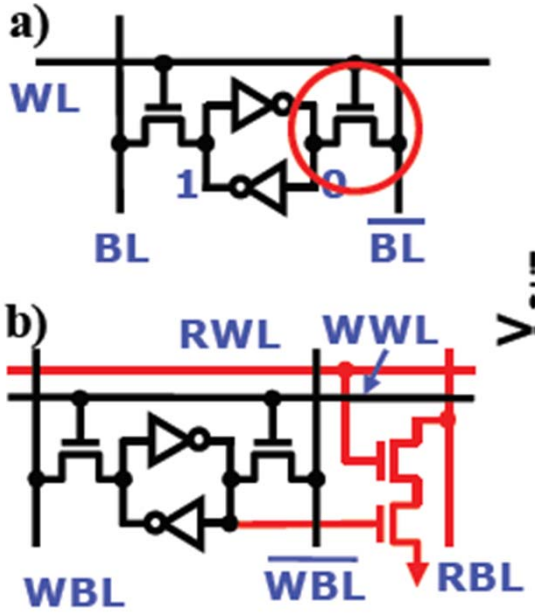
- 4T cell – “A Reusable Embedded DRAM Macrocell”, P.W.Diodato J.T.Clemens W.W.Troutman W.S.Lindenberger, IEEE 1997 Custom Integrated Circuits Conference

- 2T1D - “A Novel Dynamic Memory Cell With Internal Voltage Gain”, Wing K. Luk and Robert H. Dennard, IEEE Journal of Solid-State Circuits, v. 40, n. 4, April 2005

- 3T1D – “A 3-Transistor DRAM Cell with Gated Diode for Enhanced Speed and Retention Time”, Wing K. Luk, Jin Cai, Robert H. Dennard, Michael J. Immediato, Stephen V. Kosonocky, IEEE 2006 Symposium on VLSI Circuits

Novel cell designs

- 8T cell – “L. Chang, D. Fried and J. Hergenrother, “Stable SRAM cell design for the 32 nm node and beyond”, VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on, 2005, 128-129



Introducing New Cells in CACTI

- CACTI is the most commonly used memory structure characterization programs.

- In this project, you will interact and modify it to suit your needs.

Introducing New Cells in CACTI

STEPS:

1. Download CACTI 6.5 http://www.hpl.hp.com/research/cacti/
2. Install it in your system and read the documentation
3. Chose a new cell design of the ones previously proposed in this document (4T, 3T, 1T, 2T1D, 3T1D). Read about those cells, justify the cell area assumptions and implement it in CACTI (Watch out whether your cell is single or double endded!!)
4. Introduce the possibility of chosing the cell type in the command line (either the available 6T SRAM cell) or your newly designed cell.
5. Evaluate several configurations for delay (access time) and power. 8KB-2MB caches, associativities from 1 to 8, and block sizes from 32bytes to 128 bytes. (All variables increase in power of 2 steps)

Introducing New Cells in CACTI

Hand in (email) a PDF with:

1. Description of the cell implemented
2. Modifications made to CACTI
3. Evaluation of the configurations:
    1. Effect of the associativity over power and delay
    2. Effect of line-size over power and delay
    3. Effect of size over power and delay

Hand in (email) the source CACTI code.

1. Be a nice programer and clearly mark your modifications!