Technology Overview

Ramon Canal
NCD – Master MIRI

Modular Characterization

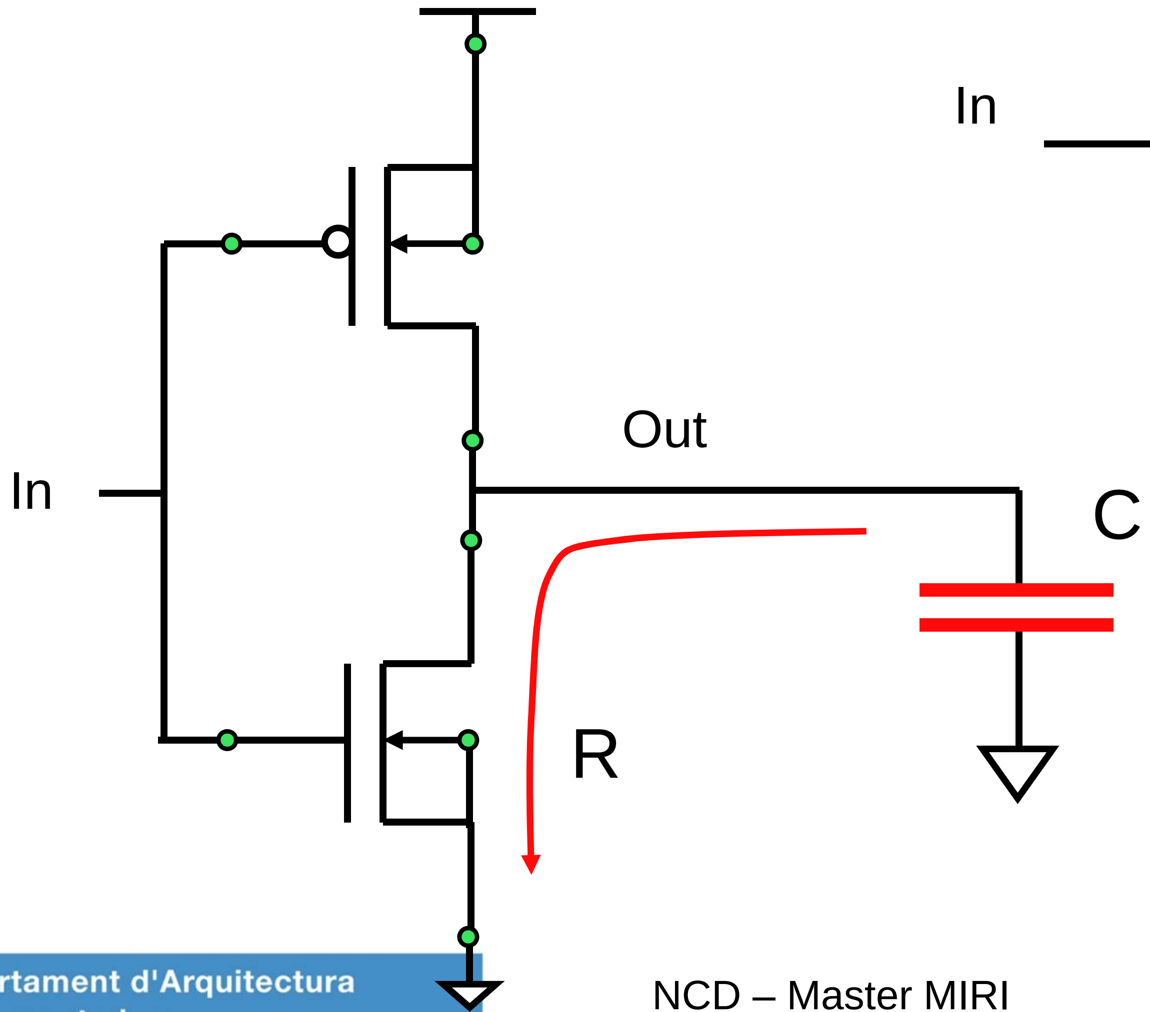
- It is impossible to analyze a million transistor circuit looking at every single transistor
- Modular approach makes it feasible
- Grouping transistors in gates, gates in blocks and so on.
- Keys to the analysis of MOS circuits:
  - The behavior depends on the input values.
  - Interface parameters: capacity of the inputs/outputs and impedance of the outputs
  - Transmission gates are a different story.

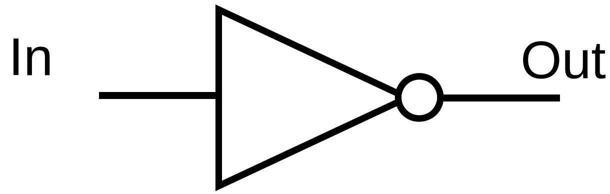
Modular Characterization

- Elements that define a module:
  - Logic function
  - Capacity of the inputs (~ gate capacity of the transistors)
  - Capacity of the outputs (~ drain capacity of the output transistors)
  - Impedance of the outputs
  - Internal propagation time
- Capacity and impedance are fixed parameters
- Internal propagation time depends on the inputs:
  - Characterize the highest/lowest times
  - Characterize depending on functionality (e.g. ALU), statistical or sampling (e.g. FU inputs), etc.

MOS gate delay

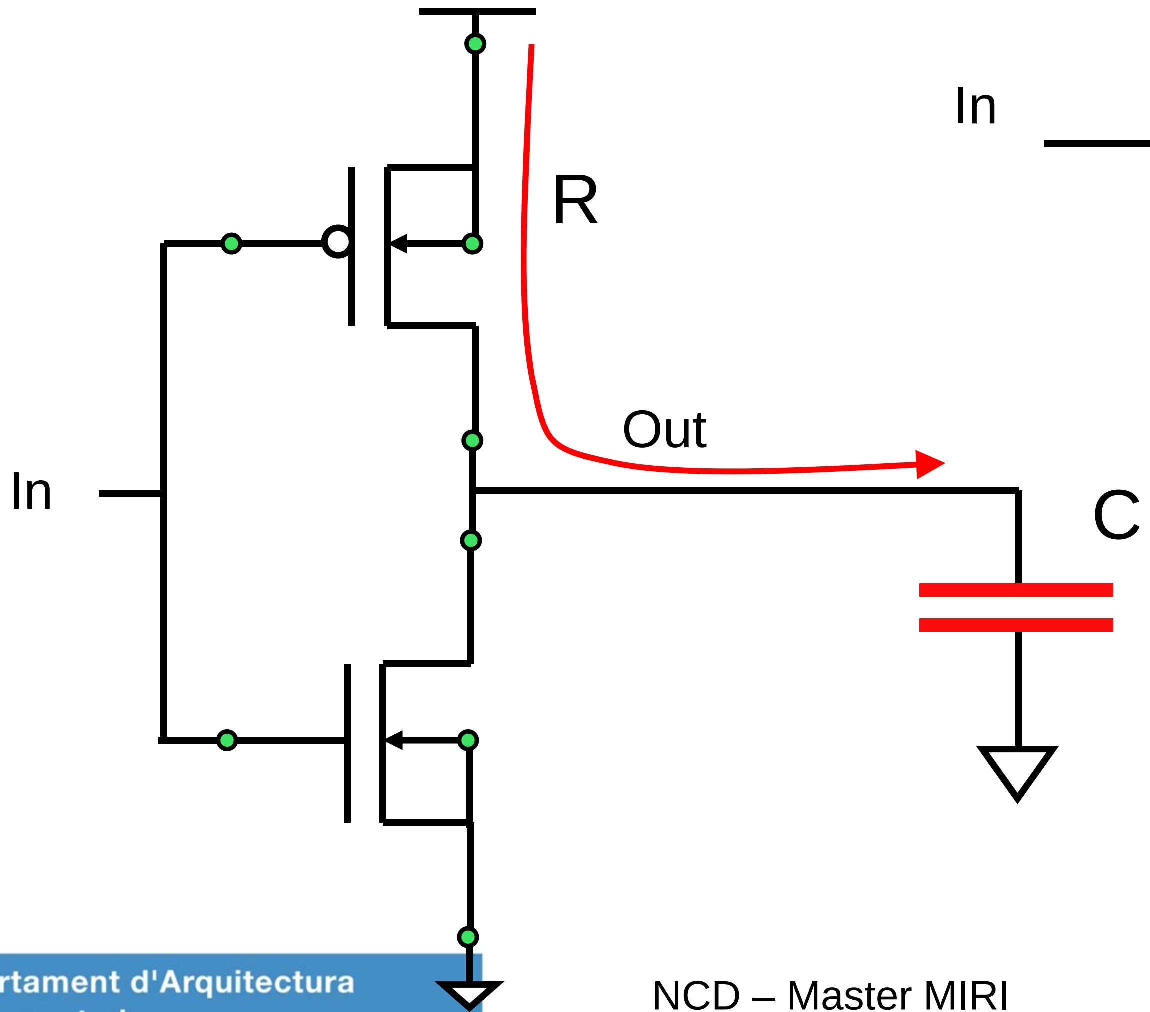
- Delay depends on RC relationship:

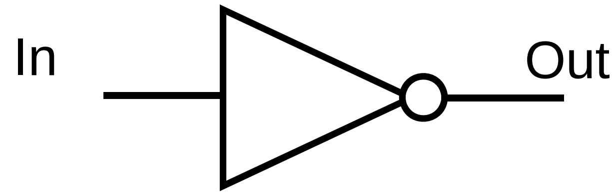




MOS gate delay

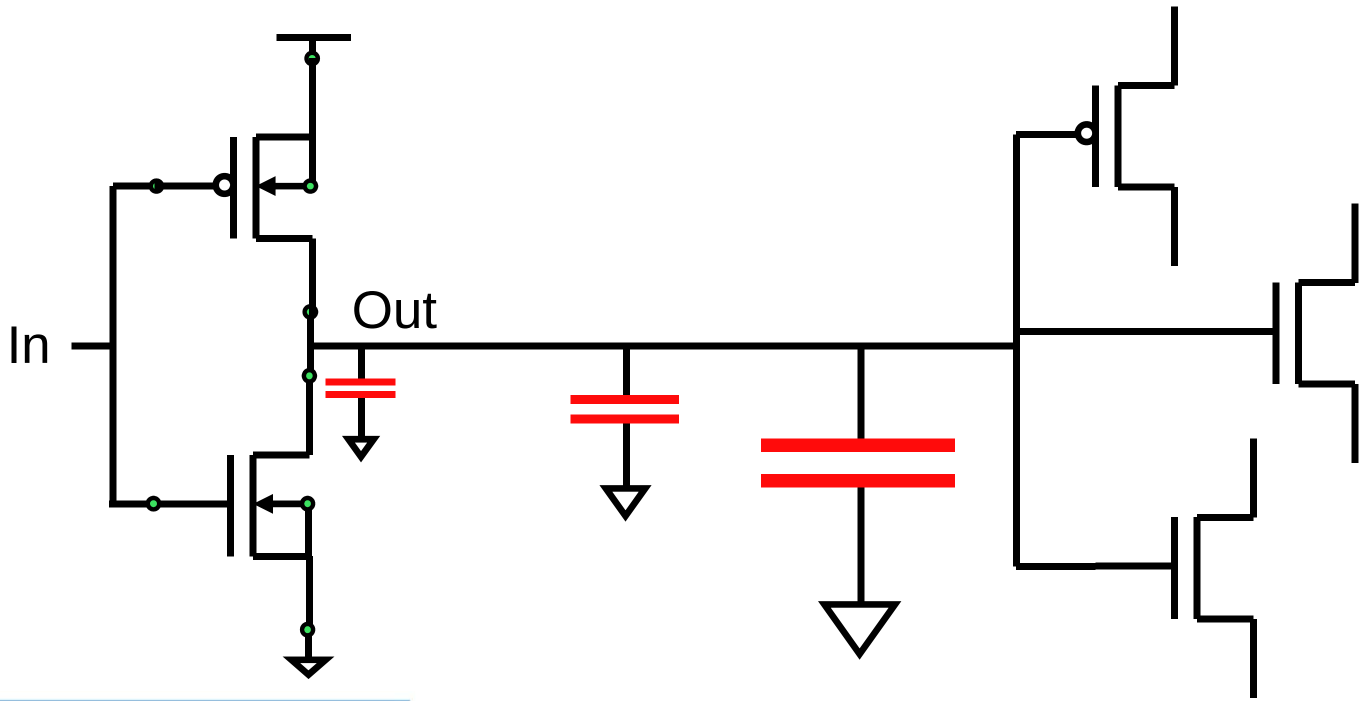
- Delay depends on the RC relationship:





MOS gate delay

- The capacity C depends on:
  - Capacity of the difussions of the output nodes
  - Capacity of the connections
  - Capacity of the nodes connected to the output

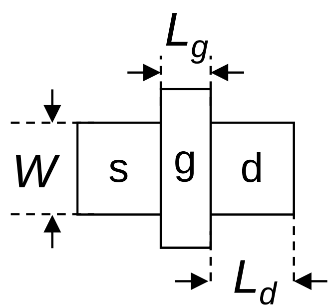


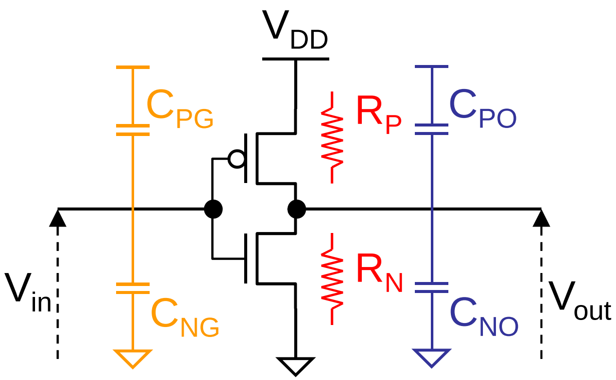
MOS gate delay

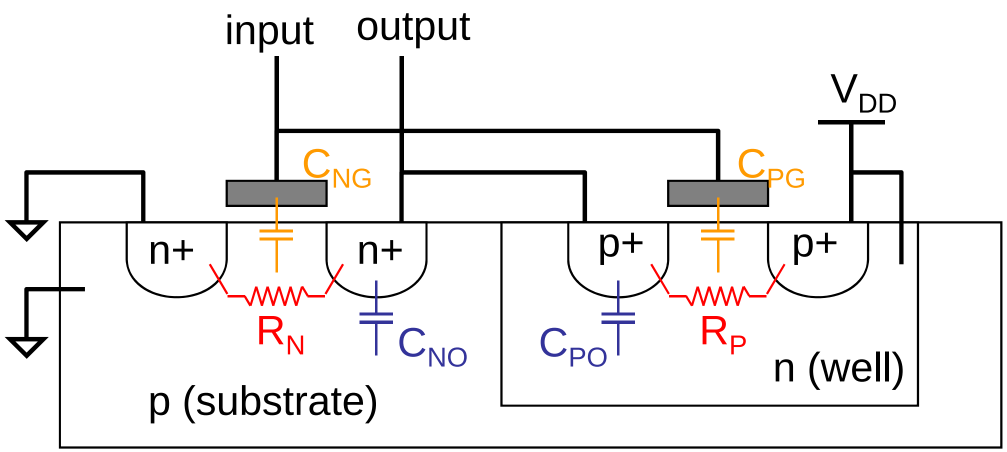
INV device model

- R_N, R_P : ON-resistance of nMOS / pMOS
  - → Proportional to L_g / W
- C_{NG}, C_{PG} : Gate capacitance of nMOS / pMOS
  - → Proportional to $L_g \cdot W$
- C_{NO}, C_{PO} : Drain capacitance of nMOS / pMOS
  - → Proportional to $L_d \cdot W$ and $L_d + W$
- ➢ *In reality, R_N, R_P, C_{NO}, C_{PO} are not constant, but dependent on the voltages at the gate and drain*

MOS layout

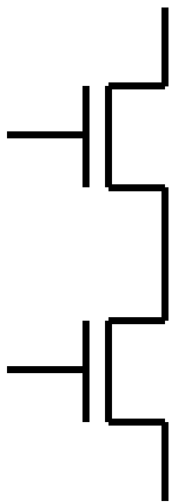


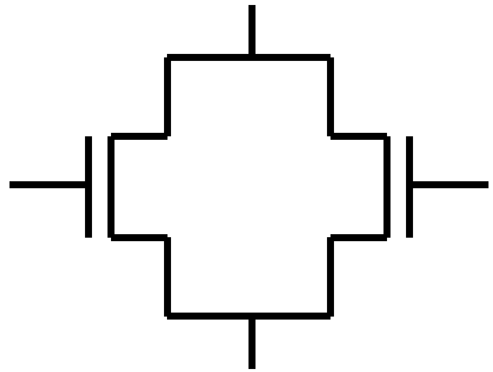




MOS gate delay

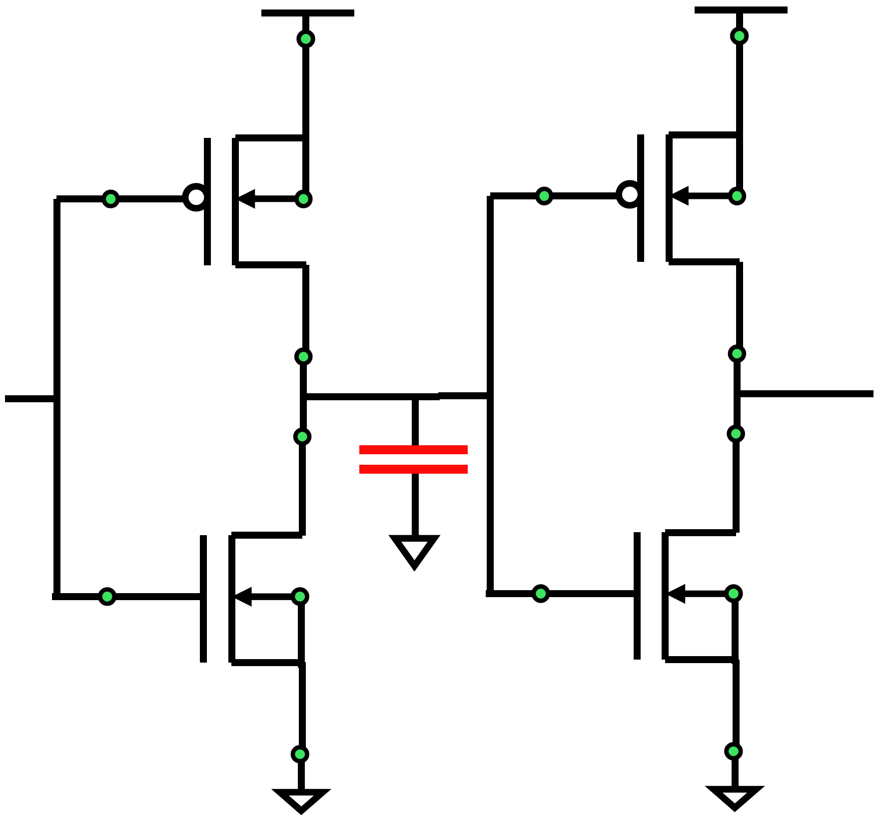
- The resistance R depends on:
  - Dimensions of the transistors that charge/discharge the output capacity (~ L/W).
  - Transistors in a row add resistance: L_1/W_1 L_2/W_2
    - $R \sim L_1/W_1 + L_2/W_2$
  - Transistors in parallel reduce resistance: L_1/W_1 L_2/W_2
    - $R \sim 1 / \left(1/(L_1/W_1) + 1/(L_2/W_2)\right)$

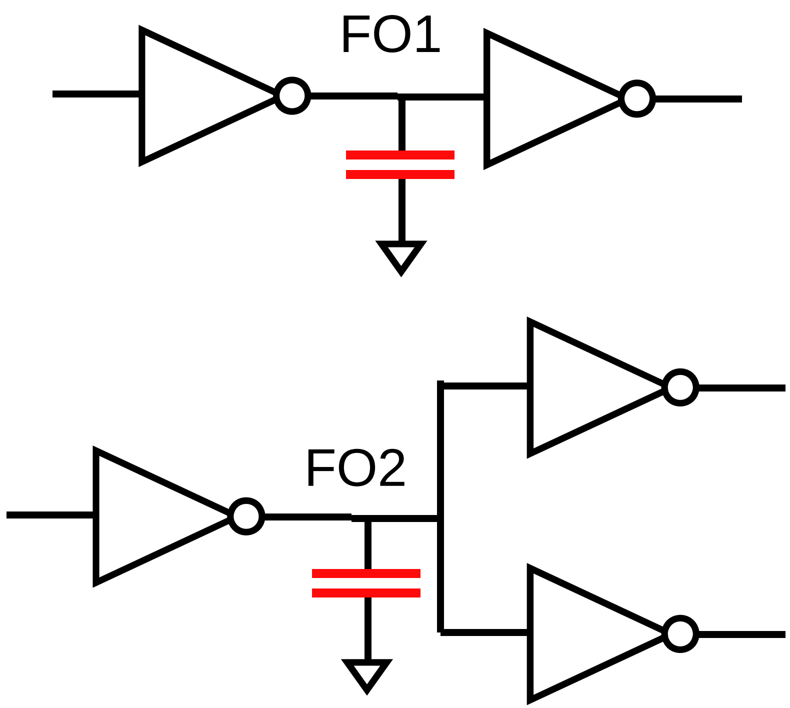




MOS gate delay

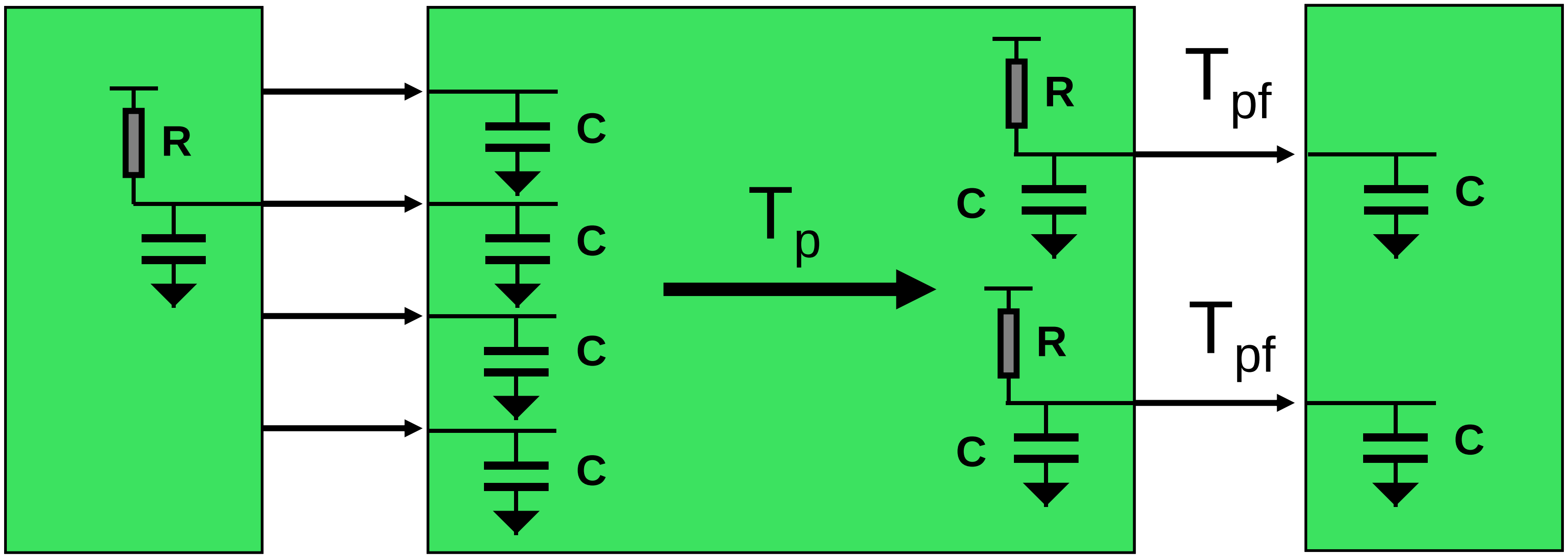
- FO1 (Fan Out of 1) is defined as the delay of an inverter connected to another inverter of equal sizes
  - FO2 is equivalent to connecting two inverters, etc.





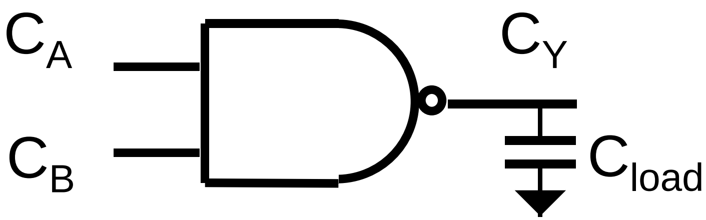
Characterization elements

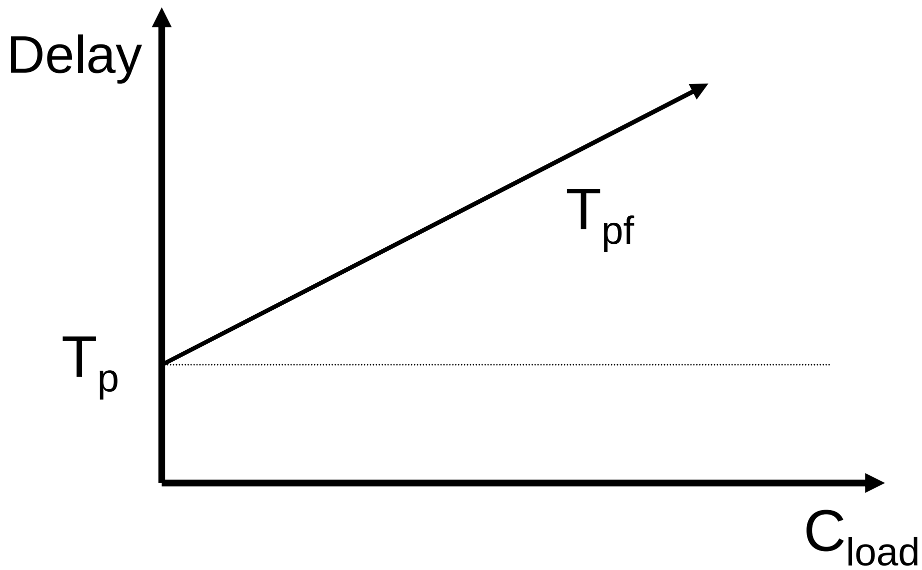
- Module parameters:
  - Capacity of the inputs: C_I
  - Capacity of the outputs: C_O
  - Impedance of the outputs.
    Charge-dependant propagation time: T_{pf}
  - Internal propagation time: T_p



Example: characterization of a NAND

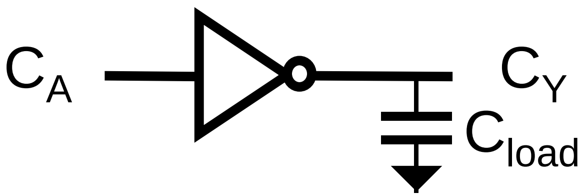
- Parameters of the gate **NAND2**
  - Input Capacity: C_{I-A} C_{I-B} 40 fF
  - Output Capacity : C_{O-Y} 25 fF
  - Propagation times:
    - Charge-dependant: $T_{pf\ Y}$ 0.02 ns/fF
    - Internal: $T_{p\ Y}$ 1 ns

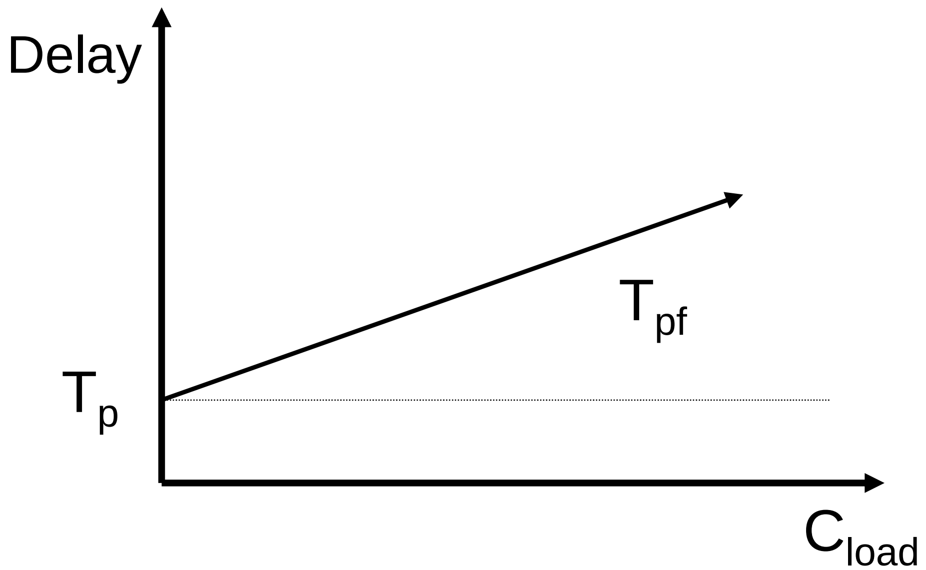




Example: characterizing an inveter

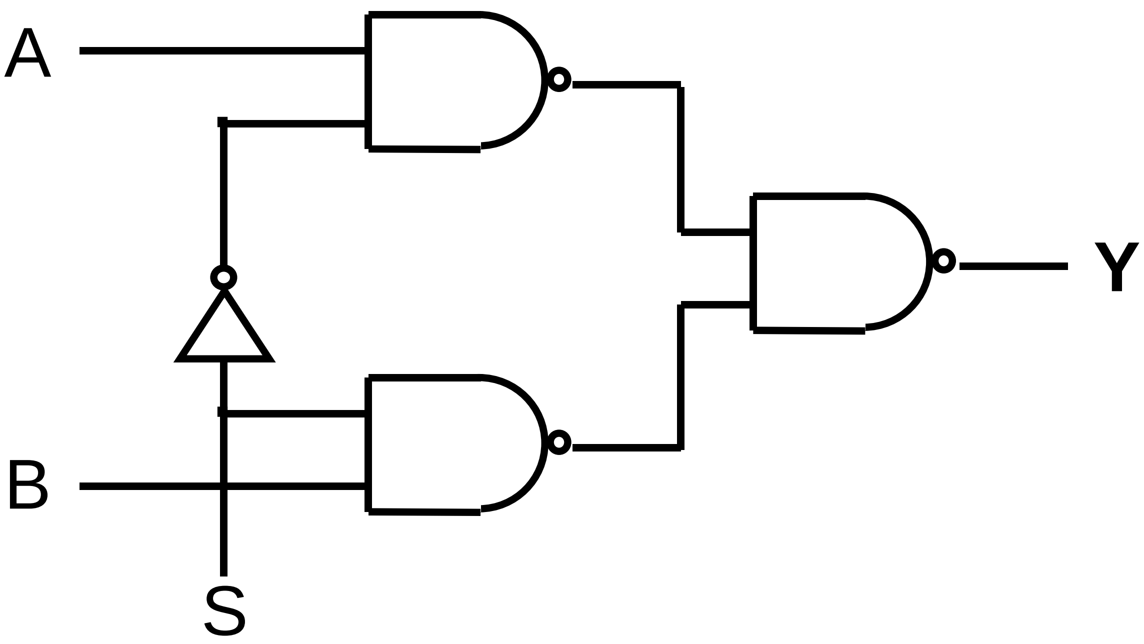
- Parameters of the gate: **INV**
  - Input Capacity: $C_{I\text{-}A}$ 30 fF
  - Output Capacity: $C_{O\text{-}Y}$ 25 fF
  - Propagation times:
    - Charge dependant: $T_{pf\ Y}$ 0.01 ns/F
    - Internal: $T_{p\ Y}$ 0.8 ns

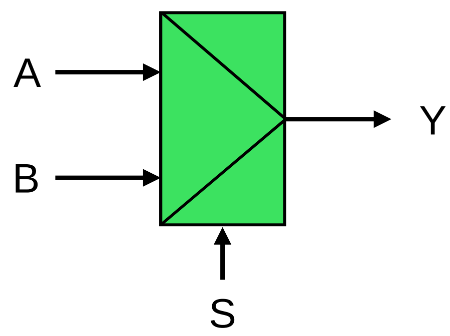




Example: characterization of a MUX

- We can analyze the MUX with both previous gates (NAND and INV):
  - **Simplicity**: we use/generate the same parameters
  - **Conservative analysis**: we introduce some error.

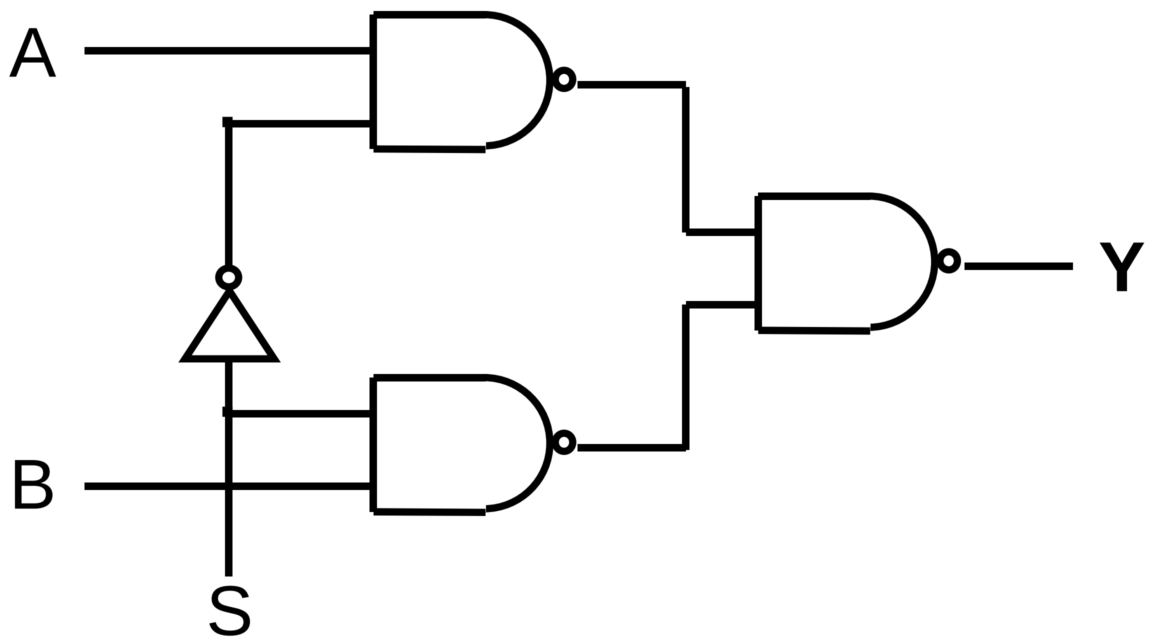


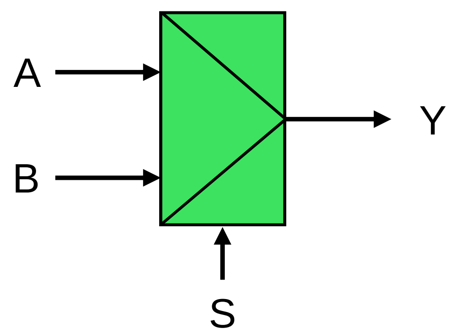


Capacity Characterization

- Capacities:
  - $C_A = C_{I\text{-}NAND} = 40fF$
  - $C_S = C_{I\text{-}NAND} + C_{I\text{-}NOT} = 70fF$

  $C_B = C_{I\text{-}NAND} = 40fF$
  $C_Y = C_{O\text{-}NAND} = 25fF$

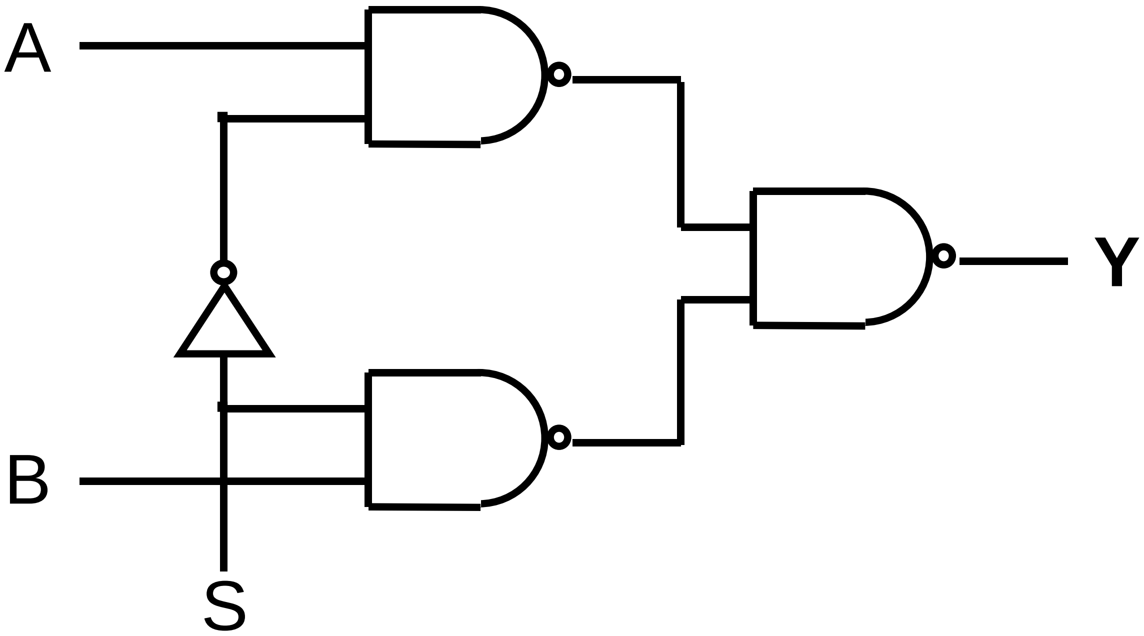


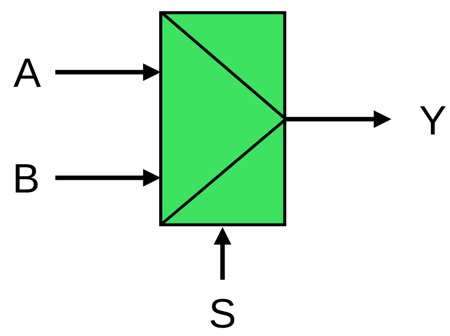


Characterization of the T_{pf}

- Charge dependant propagation time:
  - $T_{pf\ Y} = T_{pf\ NAND} = 0.02ns/fF$
  - Separating charge/discharge:

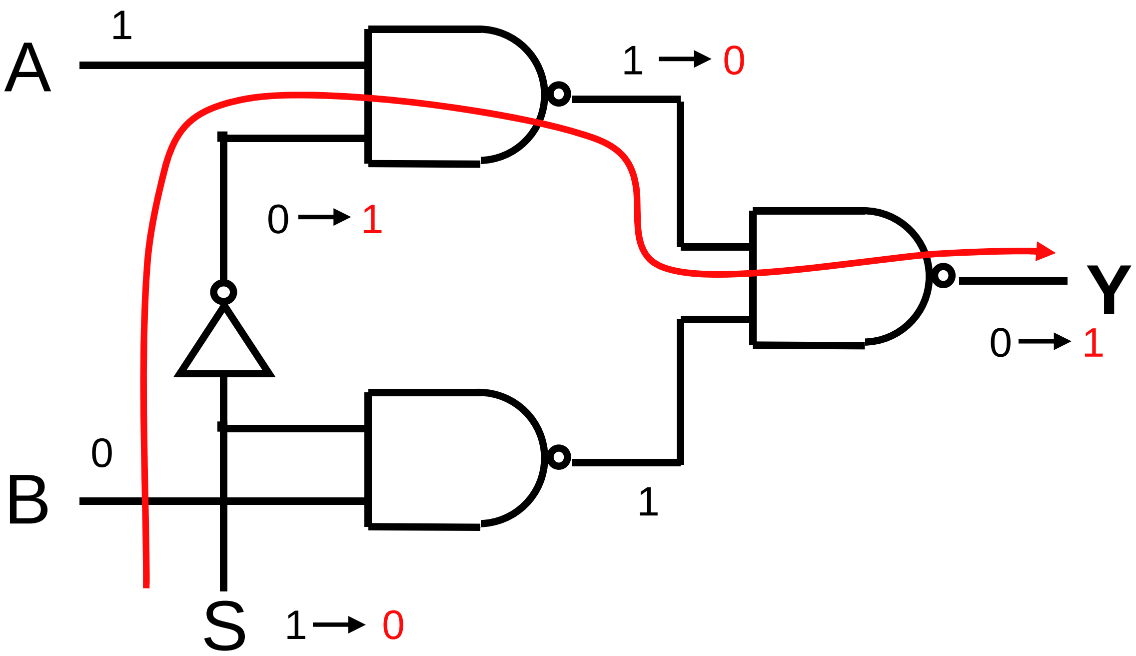
    $T_{pf\ Y+} = T_{pf\ NAND+}$ $T_{pf\ Y-} = T_{pf\ NAND-}$

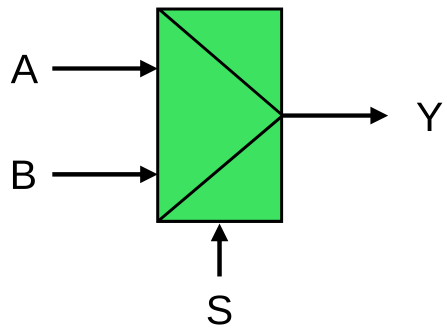




Characterization of the critical Tp

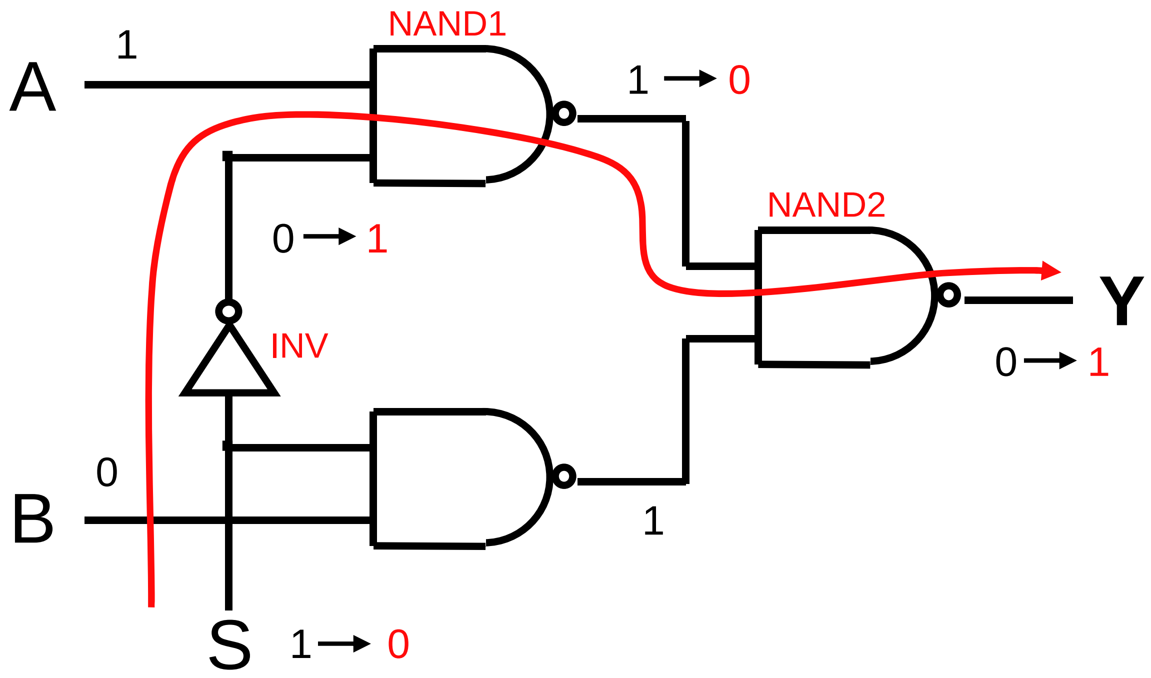
- Internal propagation time:
  - Depends on the critical path: slowest path between one input and the output of the circuit.
  - It MUST exhist (the combination of inputs is feasible)

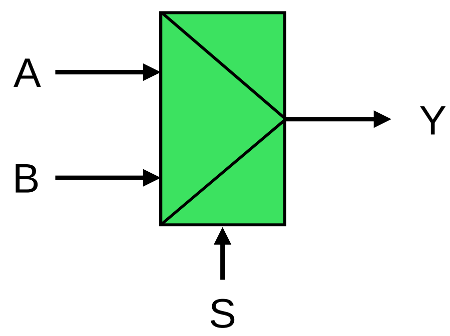




Characterization of the critical Tp (cont.)

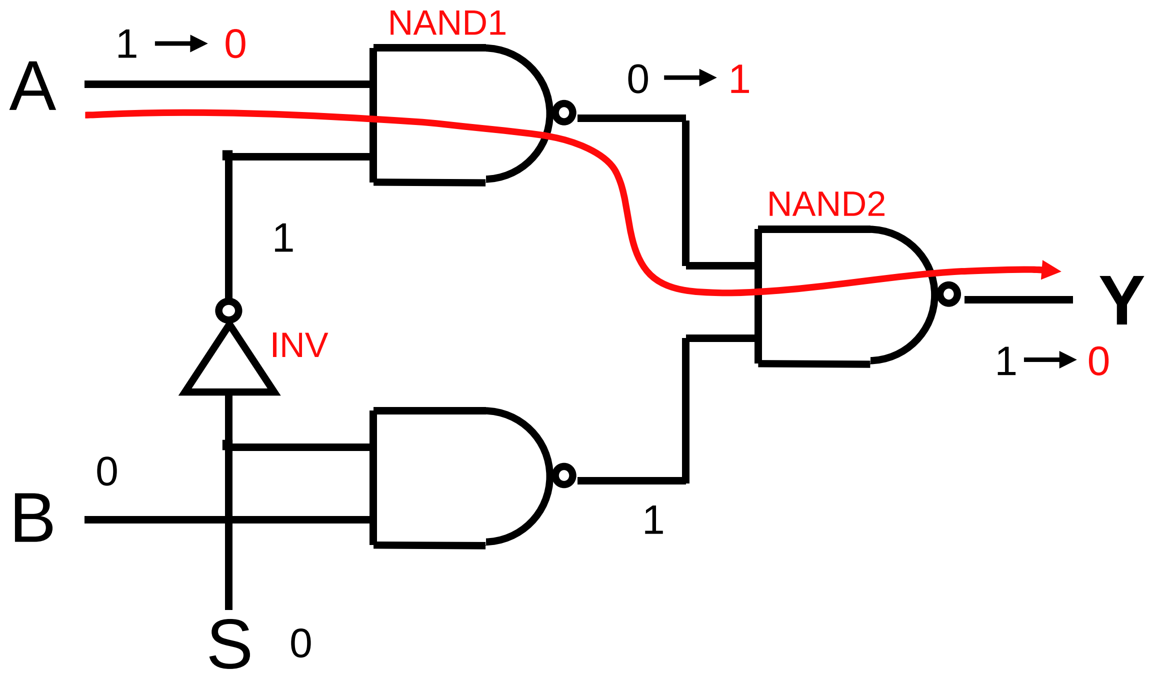
- Maximum (critical) propagation time calculation:
  - $T_{p\ Y} =$ $T_{p\ INV} + T_{pf\ INV}\ C_{I\text{-}NAND1} +$
    $T_{p\ NAND1} + T_{pf\ NAND1}\ C_{I\text{-}NAND2} + T_{p\ NAND2}$

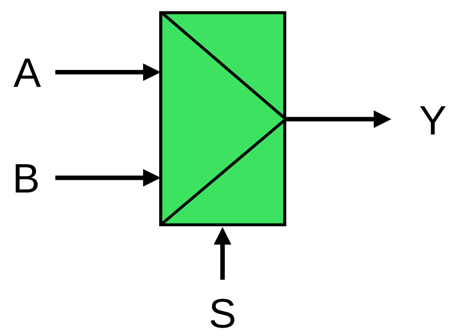




Characterization of the minimum Tp

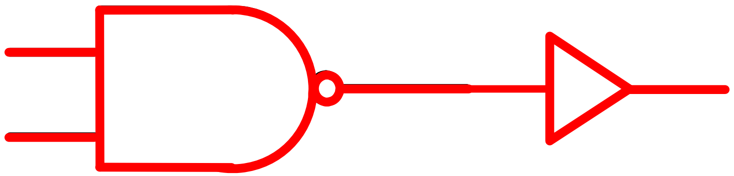
- Minimum propagation time calculation :
  - $T_{p\ Y} = \quad T_{p\ NAND1} + T_{pf\ NAND1}\ C_{I\text{-}NAND2} + T_{p\ NAND2}$

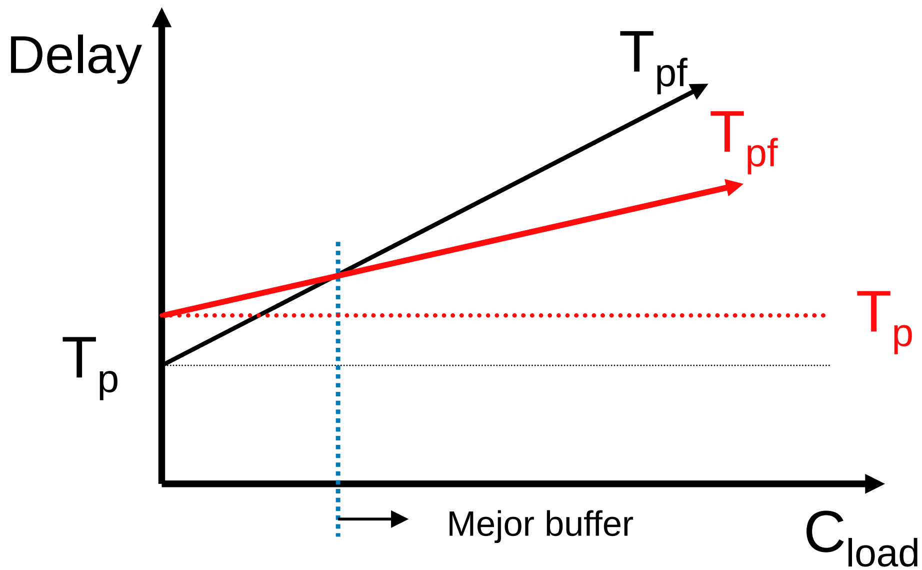




Buffers for better performance

- The delay of a component depends on its propagation time, but ALSO depends on its connection.
- We can increase overall performance by trading off T_p to reduce the T_{pf}.





Conclusions

- MOS technology allows a *modular analysis*.
- A system can be characterized with a set of parameters.
- Charge-dependant propagation times T_{pf} just depend on the output transistors.
- Buffers in the output *rise* the T_p, but *reduce* the T_{pf}.
- When considering the propagation time, there exists a high and a low, but it may not be the value we want (e.g. in a Ripple Carry Adder):
  - Critical T_p is proportional to the number of bits.
  - Usually just 4-5 bits generate carry.