

# Historical Perspective

Ramon Canal  
CTD – Master CANS



Departament d'Arquitectura  
de Computadors

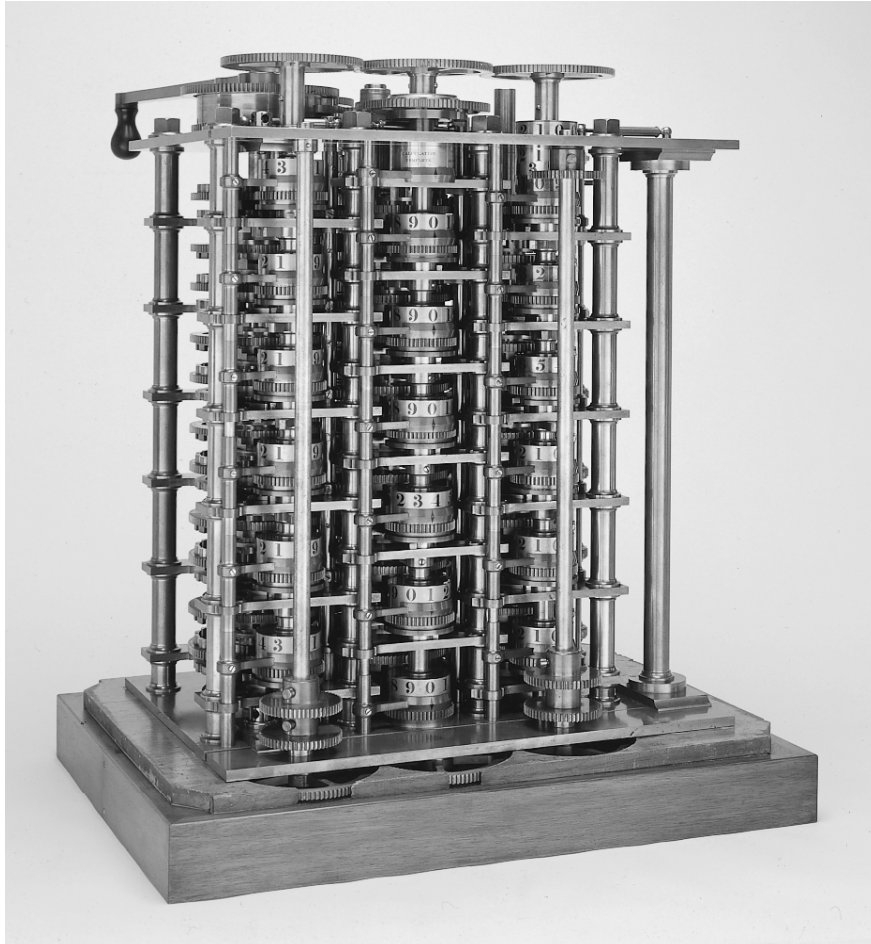
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# Agenda

- **Back in the old days**
- Back to the future



# The First Computer



**The Babbage  
Difference Engine  
(1832)**

**25,000 parts**

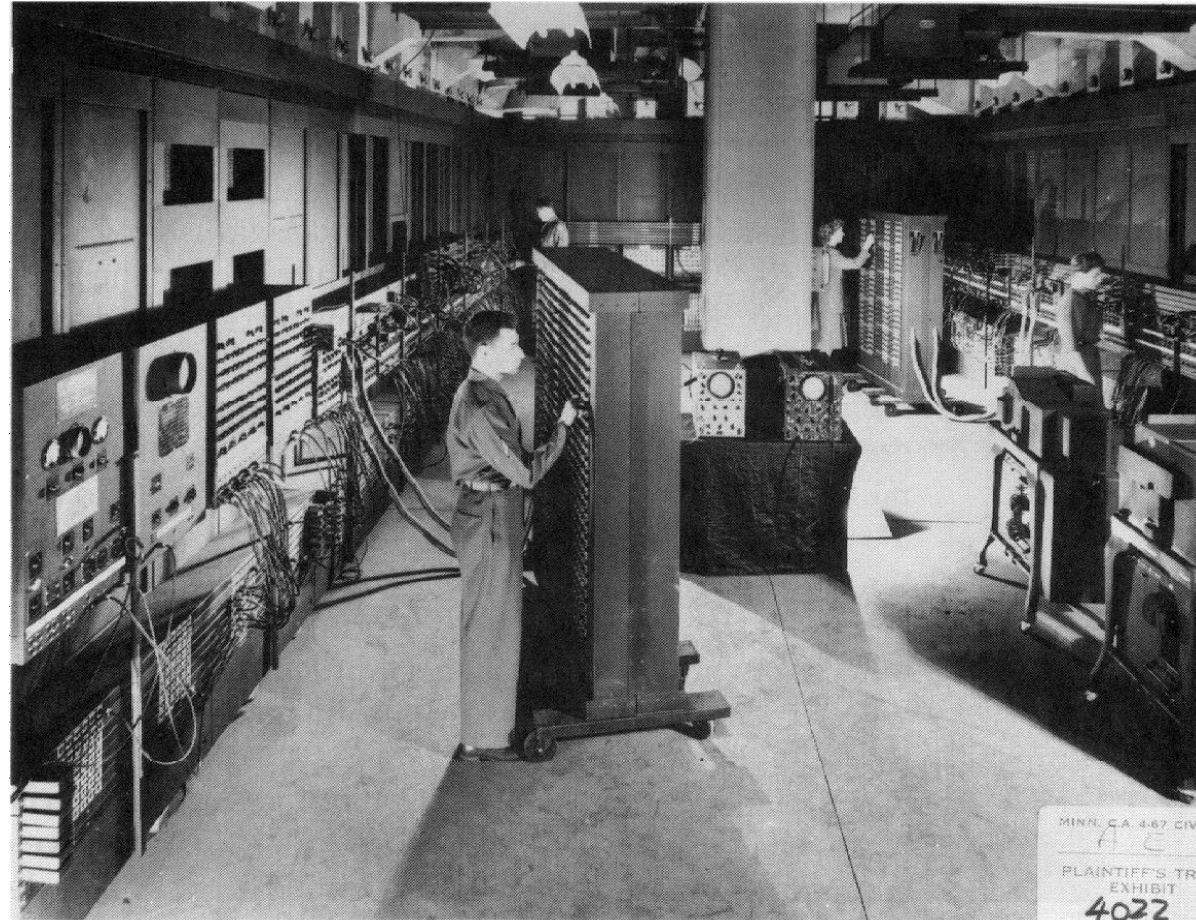
**cost: £17,470**



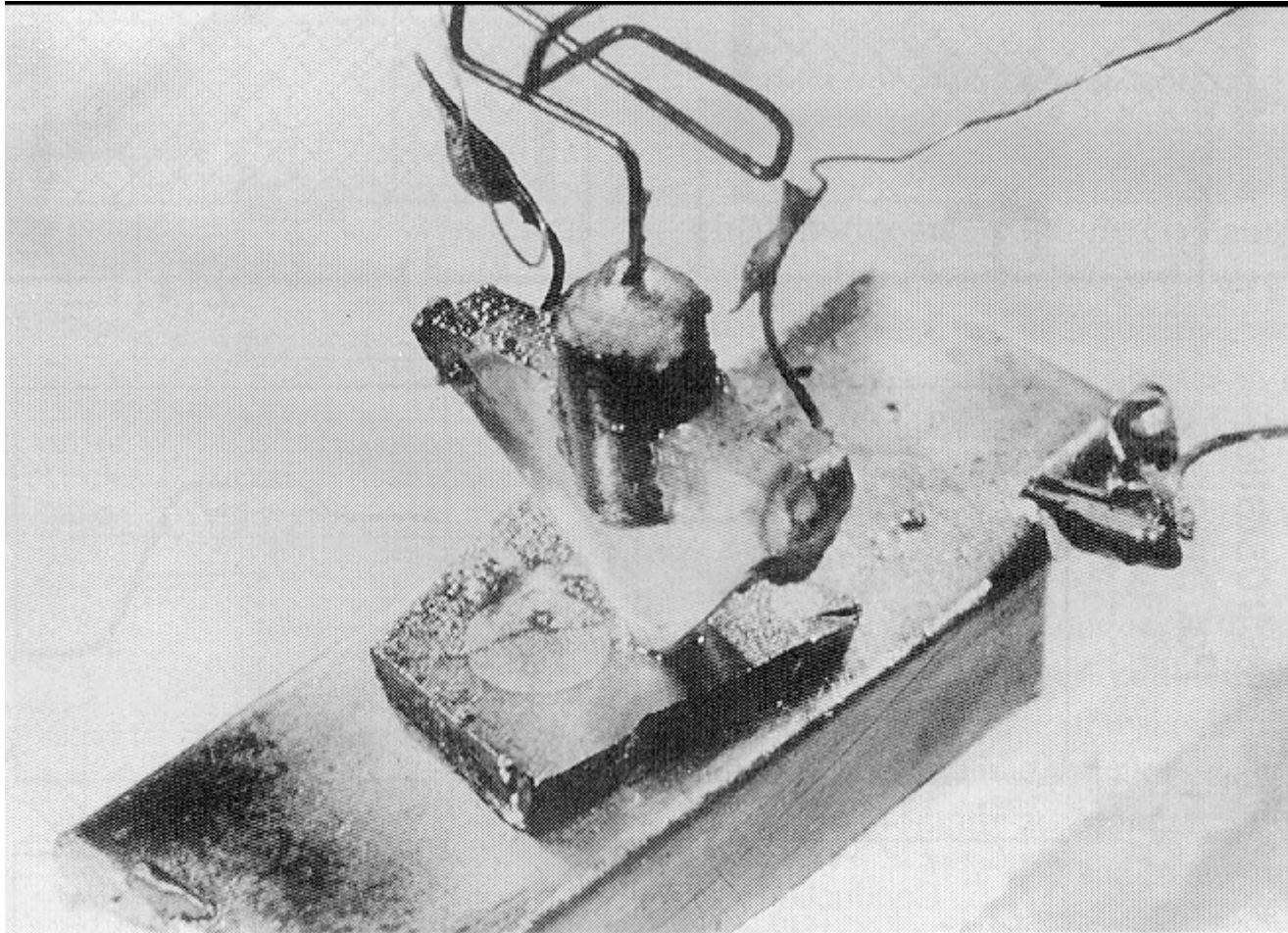
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# ENIAC - The first electronic computer (1946)

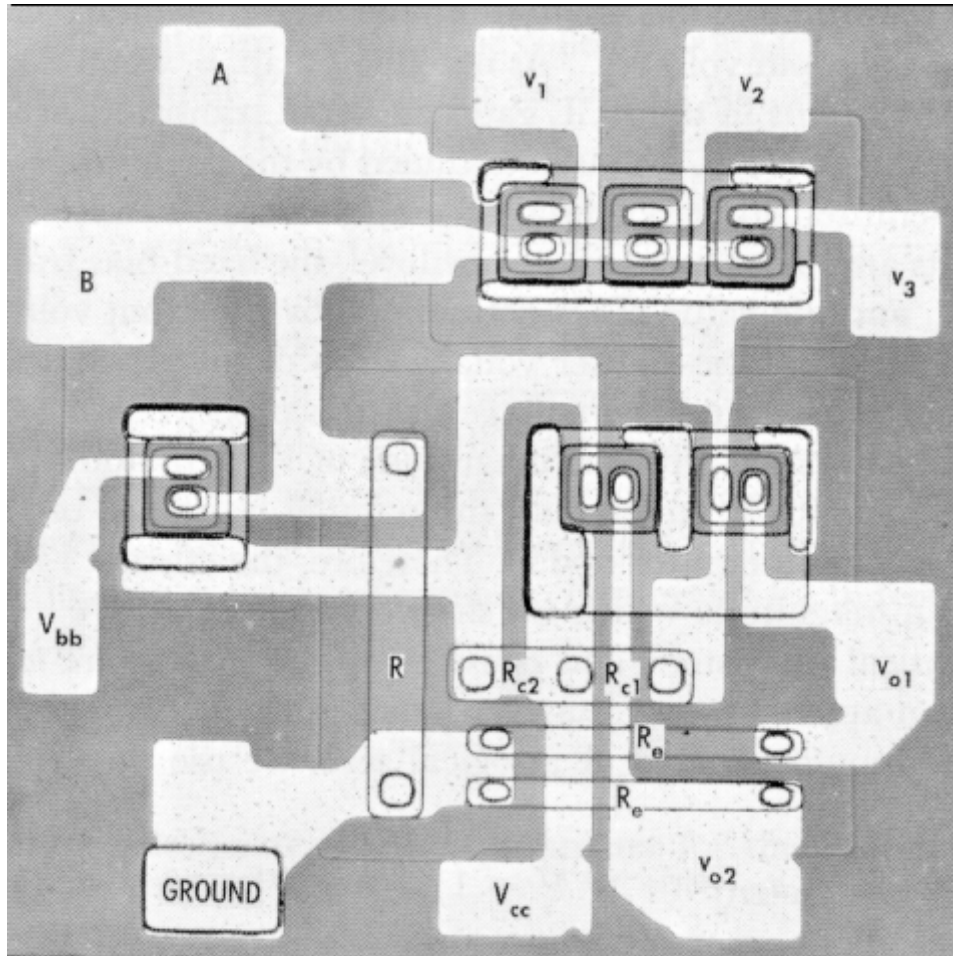


# The Transistor Revolution



First transistor  
Bell Labs, 1948

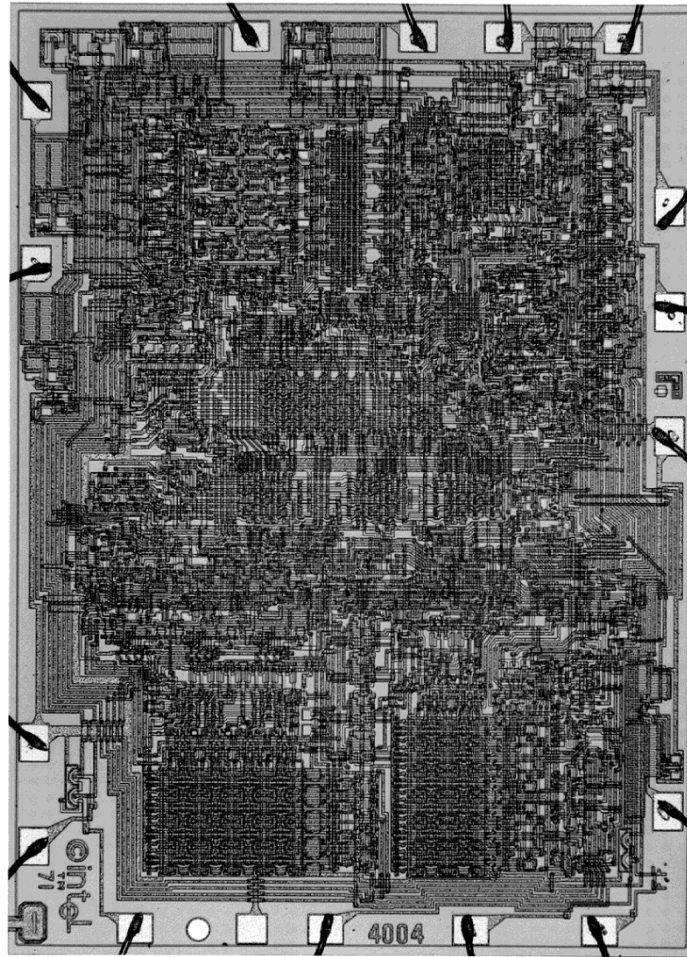
# The First Integrated Circuits



*Bipolar logic  
1960's*

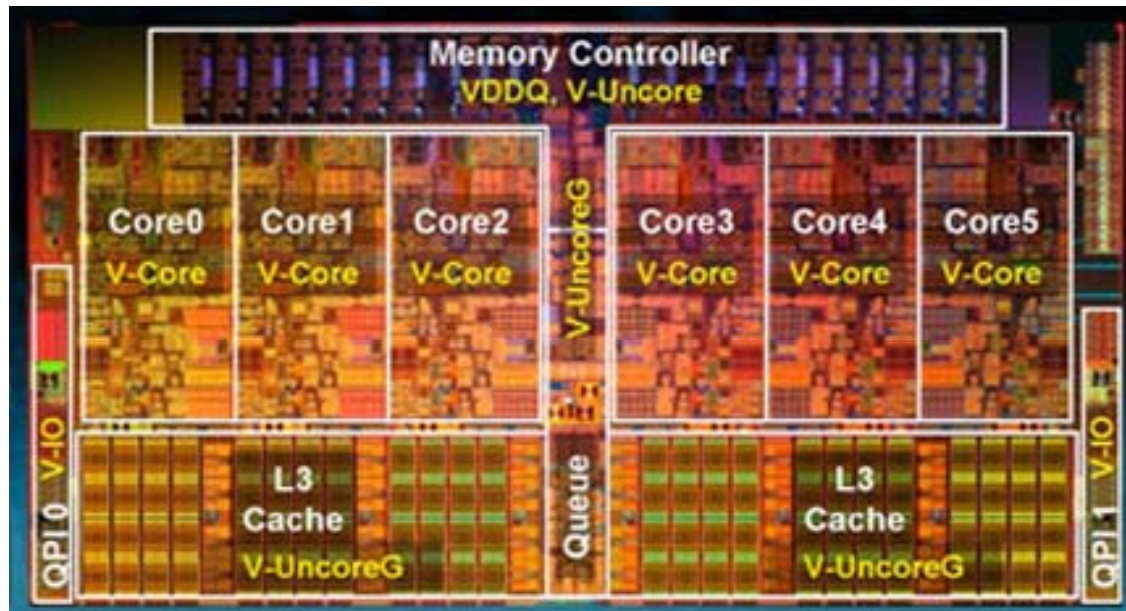
ECL 3-input Gate  
Motorola 1966

# Intel 4004 Micro-Processor



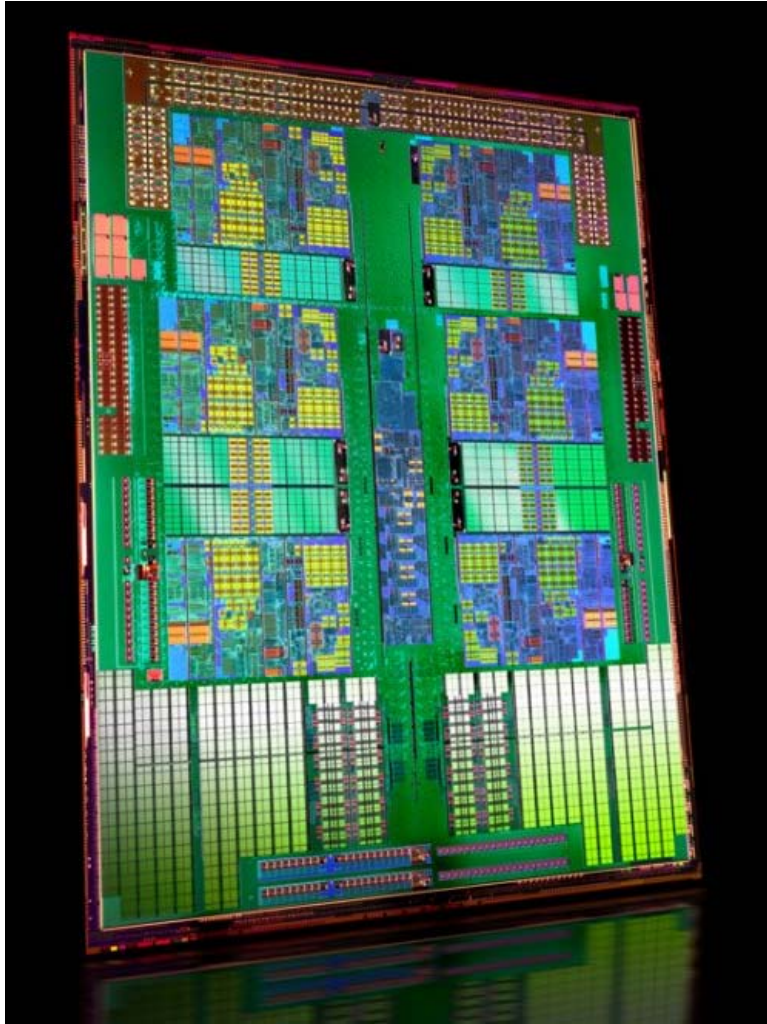
1971  
1000 NMOS transistors  
1 MHz operation

# Intel Westmere microprocessor (6C)



2010  
1'17B CMOS transistors  
~3 GHz operation  
32nm

# AMD “Istanbul” microprocessor



2009/2010  
900+M CMOS transistors  
~3 GHz operation  
45nm

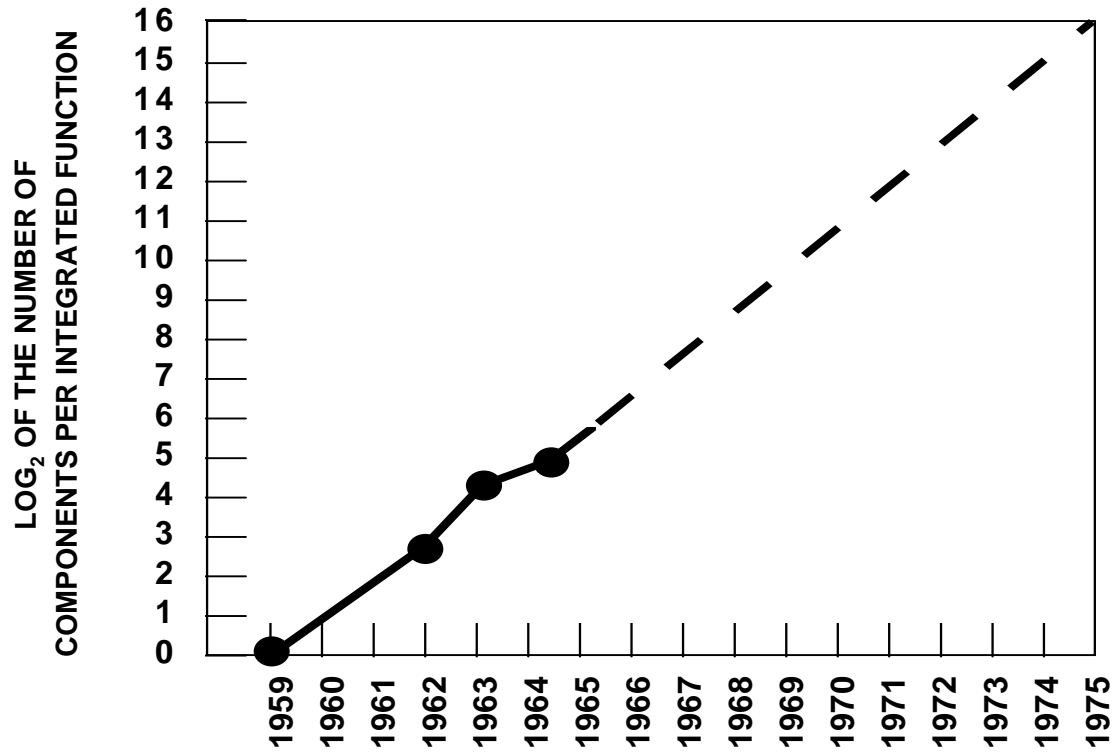


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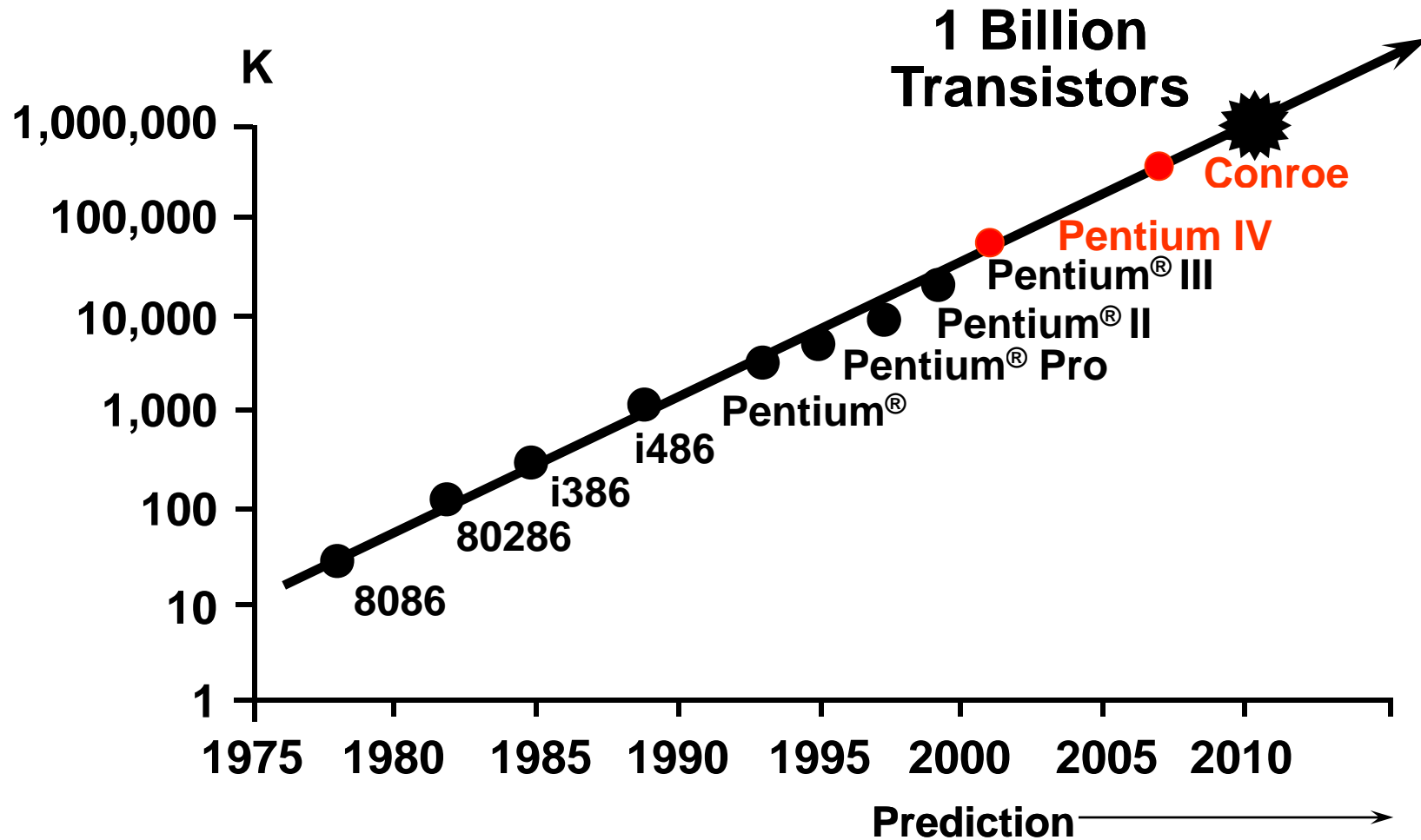
# Moore's Law



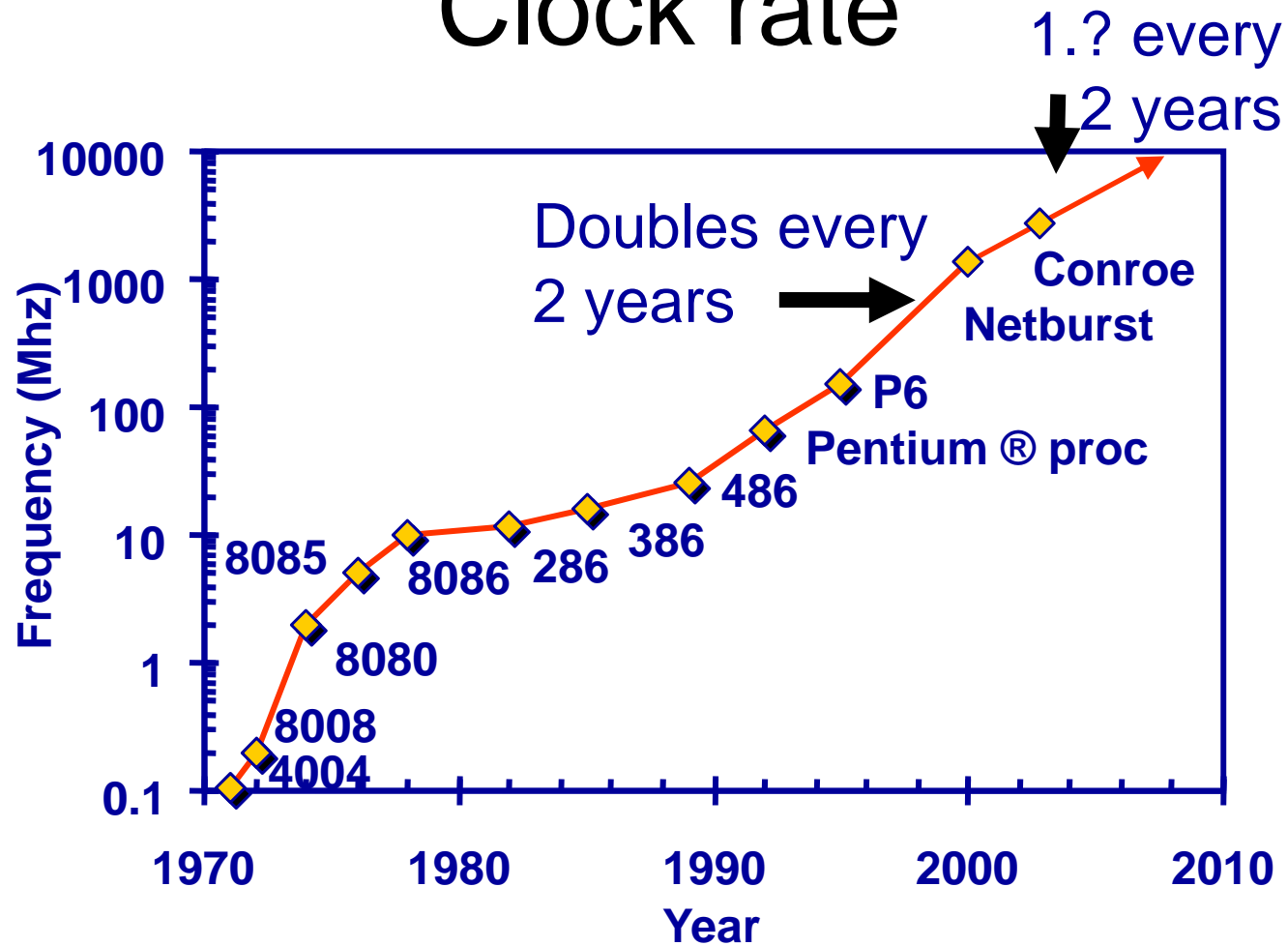
*Electronics*, April 19, 1965.



# Transistor number



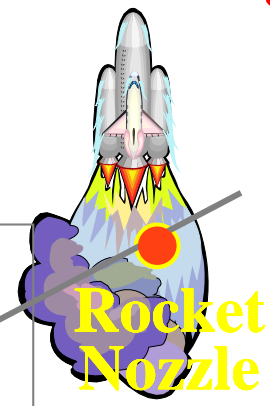
# Clock rate



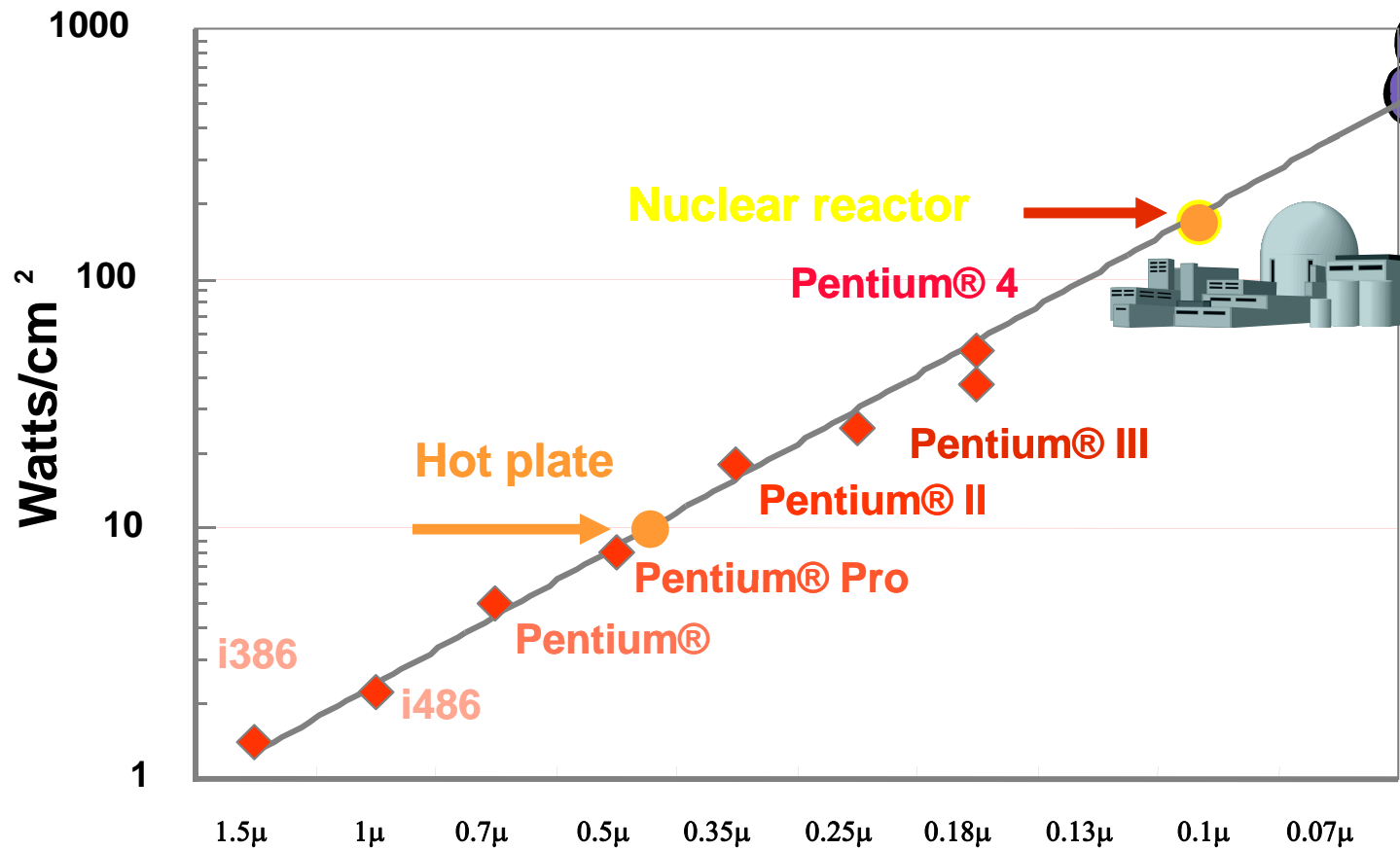
# Power Density



Sun



Rocket Nozzle



Power density is too high to keep the contacts cool enough



# Power dissipation ... for cooking?



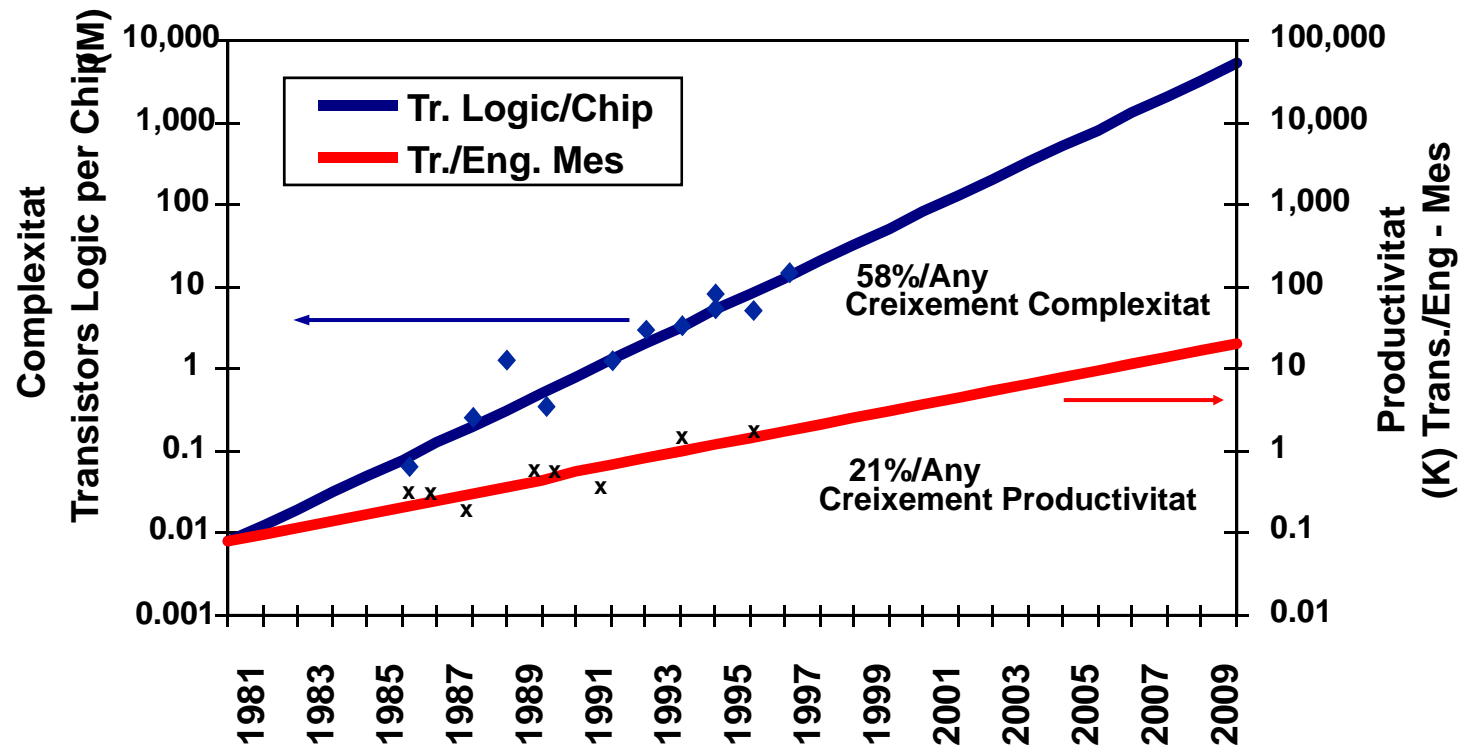


***Intel***  
***Pentium 4/2000***  
***Socket 423***  
***Intel 850 Chipset***





# Productivity Trends



Source: Sematech

**Complexity grows faster than design productivity**

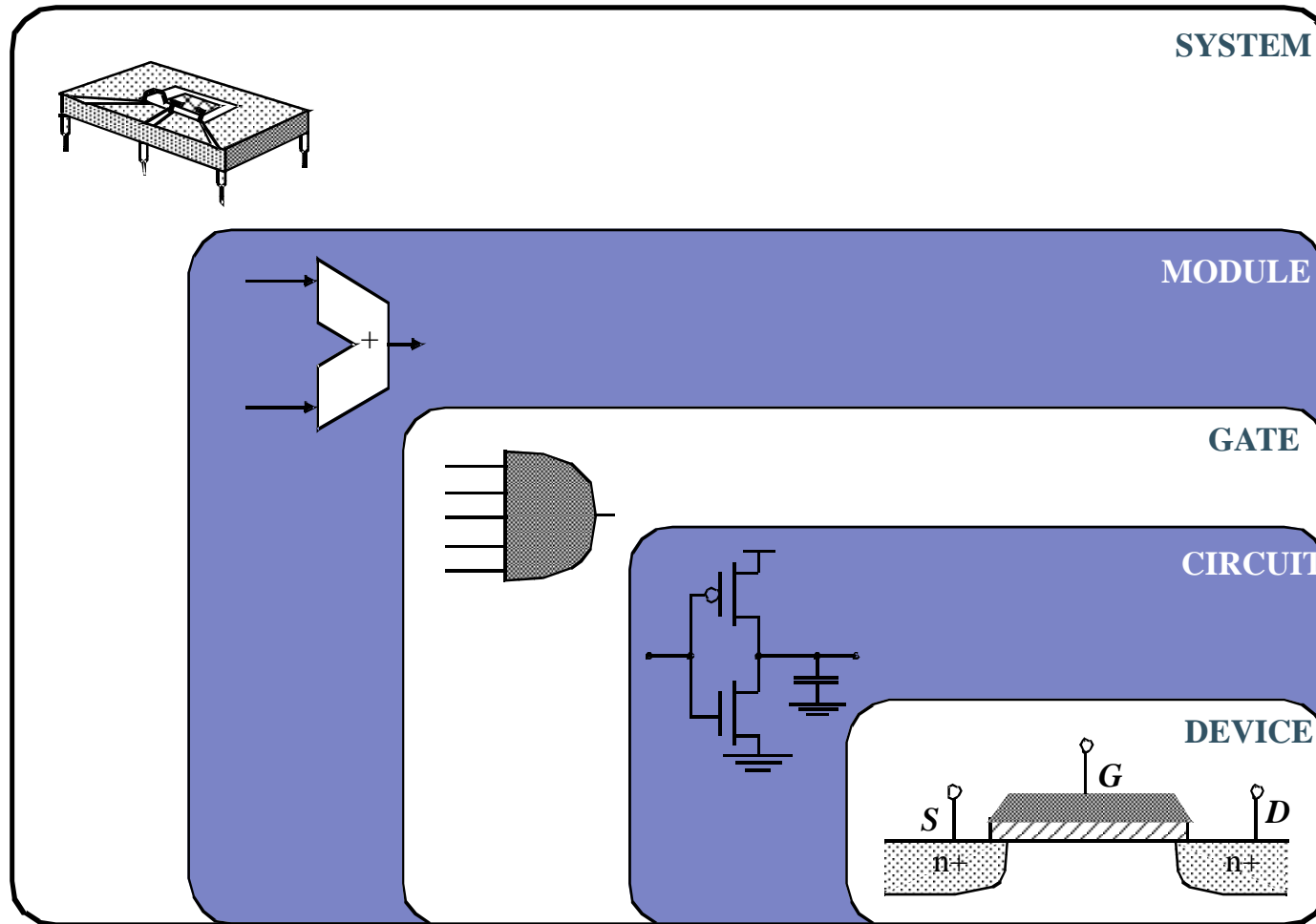


# Technology Scaling

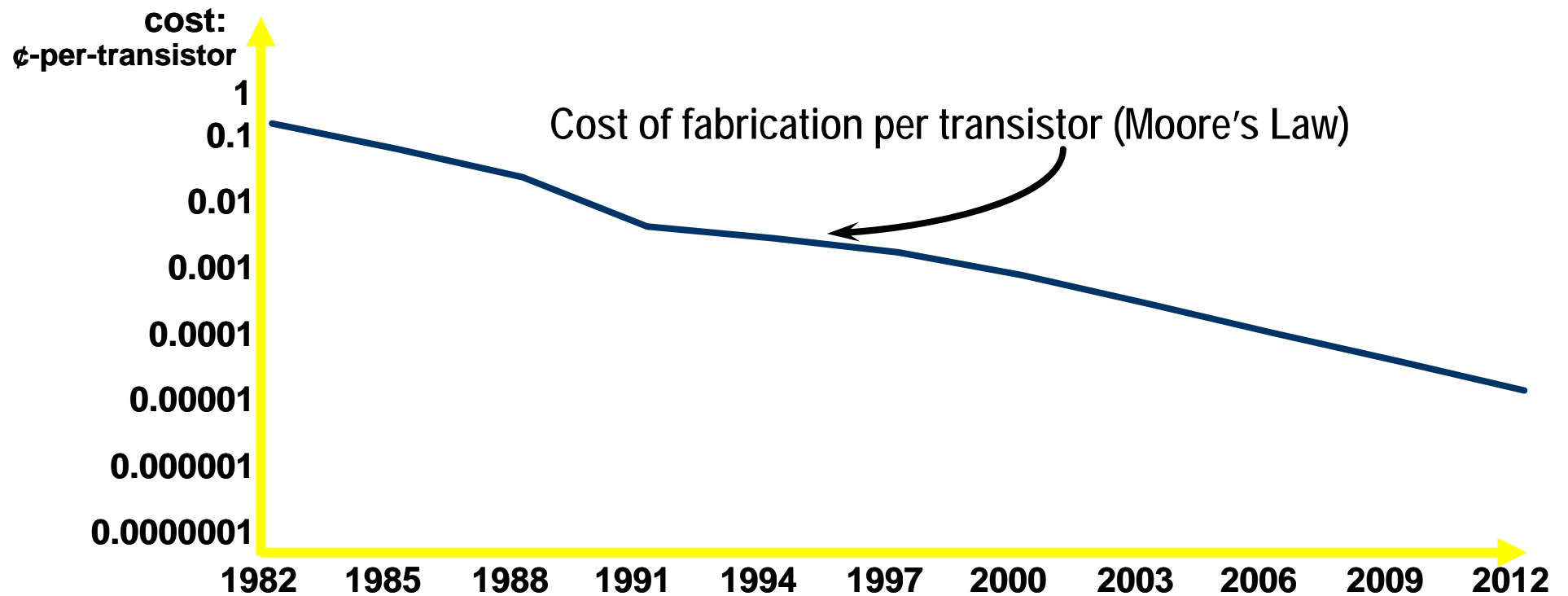
- Technology shrinks 0.7x per generation
- Each new generation can integrate 2x more functions per chip; the cost per chip is not affected significantly
- Thus... The cost per function decreases two fold
- But...
  - How can we design a chip with more functions?
  - Engineering population doesn't double every 2 years
- So: we need better and efficient design techniques:
  - Take advantage of abstraction levels



# Design Abstraction Levels



# Cost per Transistor



# Some examples (1994)

Xip	Metal Layers	Line width	Wafer Cost	Defects / cm <sup>2</sup>	Area mm <sup>2</sup>	Dies/wafer	Yield	Die cost
386DX	2	0.90	\$900	1.0	43	360	71%	\$4
486 DX2	3	0.80	\$1200	1.0	81	181	54%	\$12
Power PC 601	4	0.80	\$1700	1.3	121	115	28%	\$53
HP PA 7100	3	0.80	\$1300	1.0	196	66	27%	\$73
DEC Alpha	3	0.70	\$1500	1.2	234	53	19%	\$149
Super Sparc	3	0.70	\$1700	1.6	256	48	13%	\$272
Pentium	3	0.80	\$1500	1.5	296	40	9%	\$417

# Design tools

- VLSI system design is a complex process which requires automatization of the synthesis cycle. That's why we need design tools.
- There are three families of tools:
  - Synthesis tools
    - They allow a physical representation of circuits expressed in HDL (Hardware Definition Languages).
  - Analysis and Verification
    - They guarantee the specifications and the correctness of the design
  - Testing tools
    - They verify that there have been no errors on the fabrication process.



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