Basic CMOS structures

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NCD
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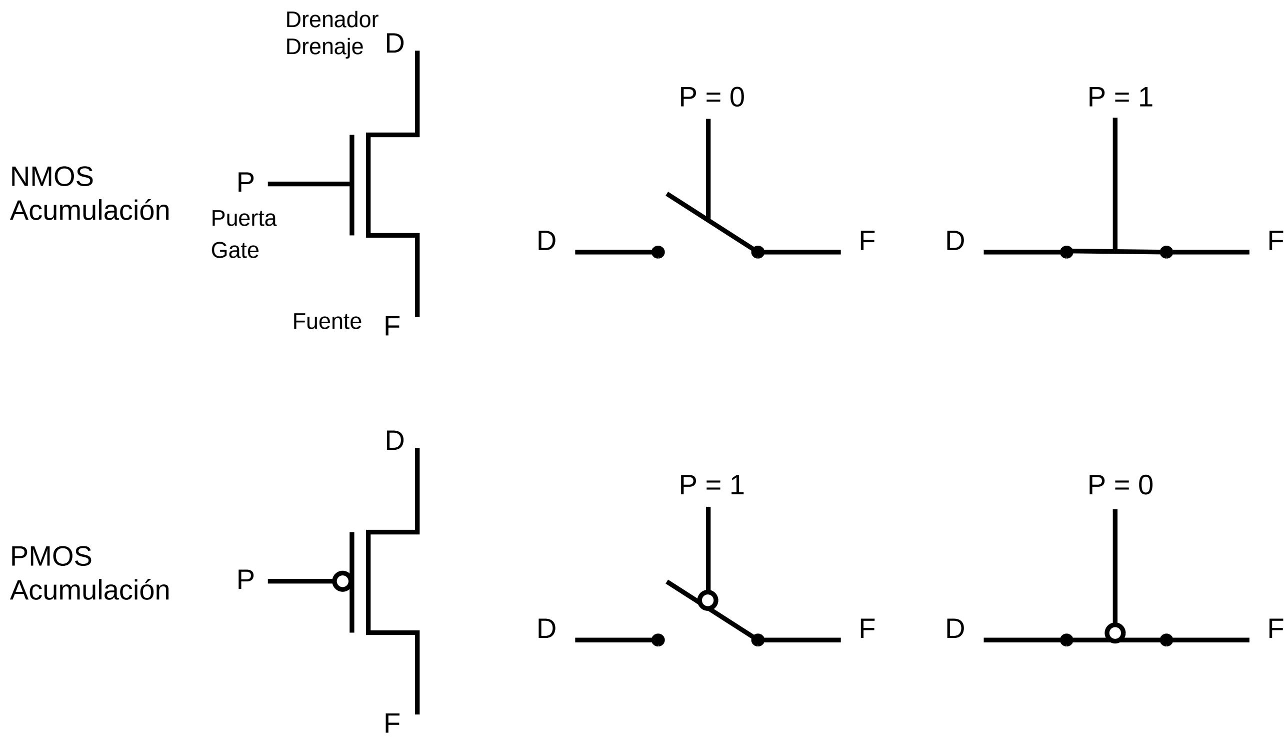
MOS: Metal Over Silicon

- Objectives:
  - Design different types of logical structures through the use of MOS Technology

- An introduction to the basic concepts of combinational logic structures

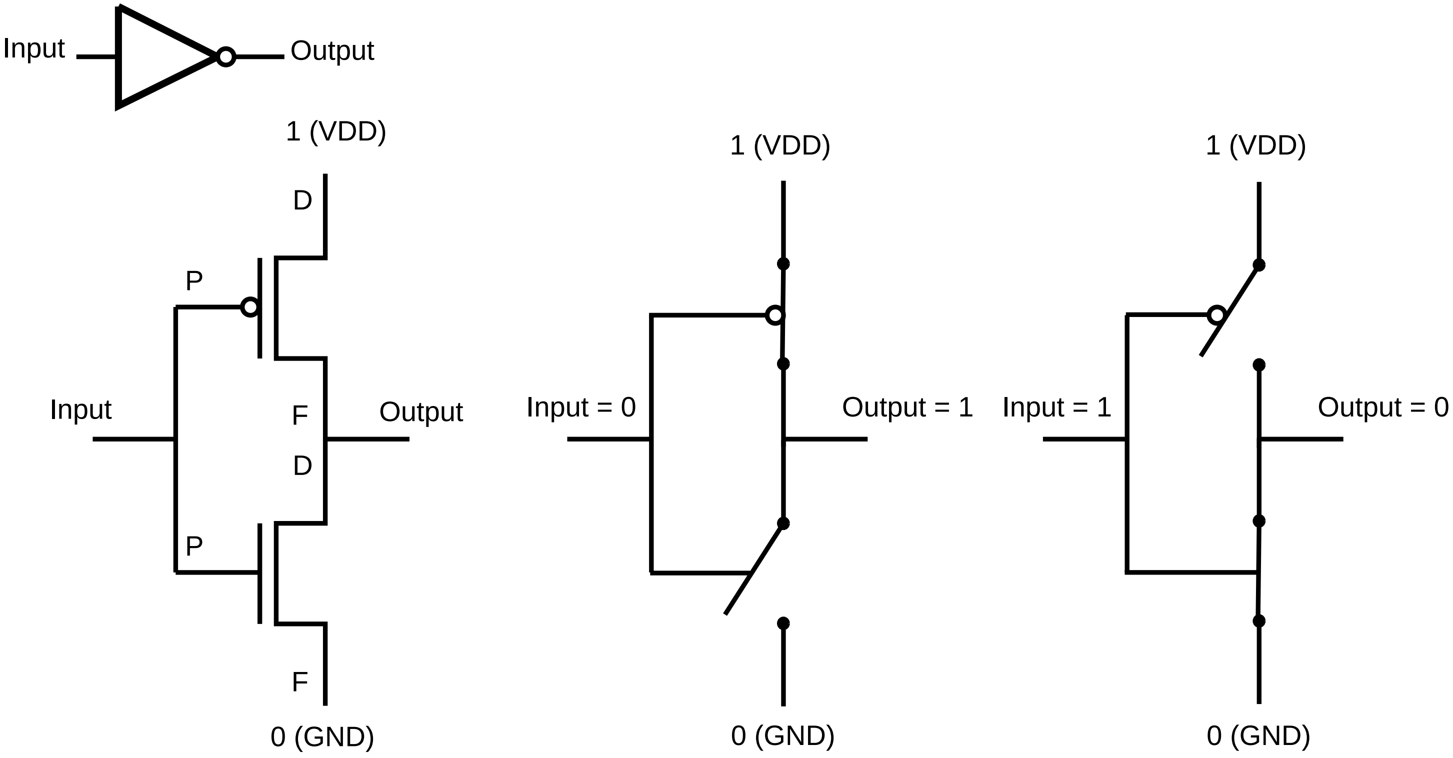
MOS Technology

- Ideal behavior: digital switch



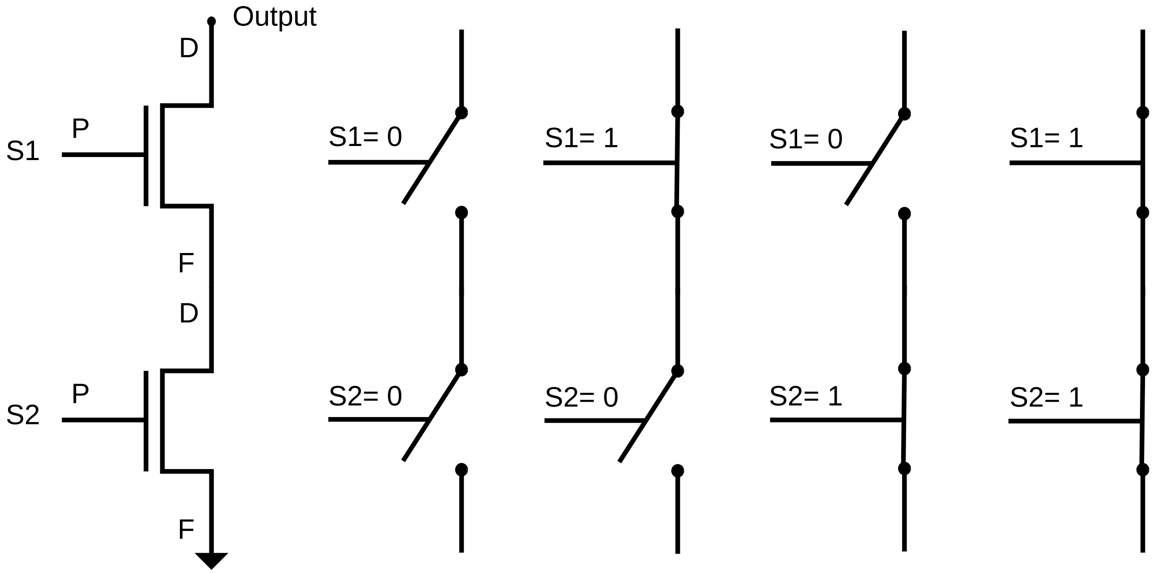
MOS Technology

- CMOS Inverter: Complementary MOS



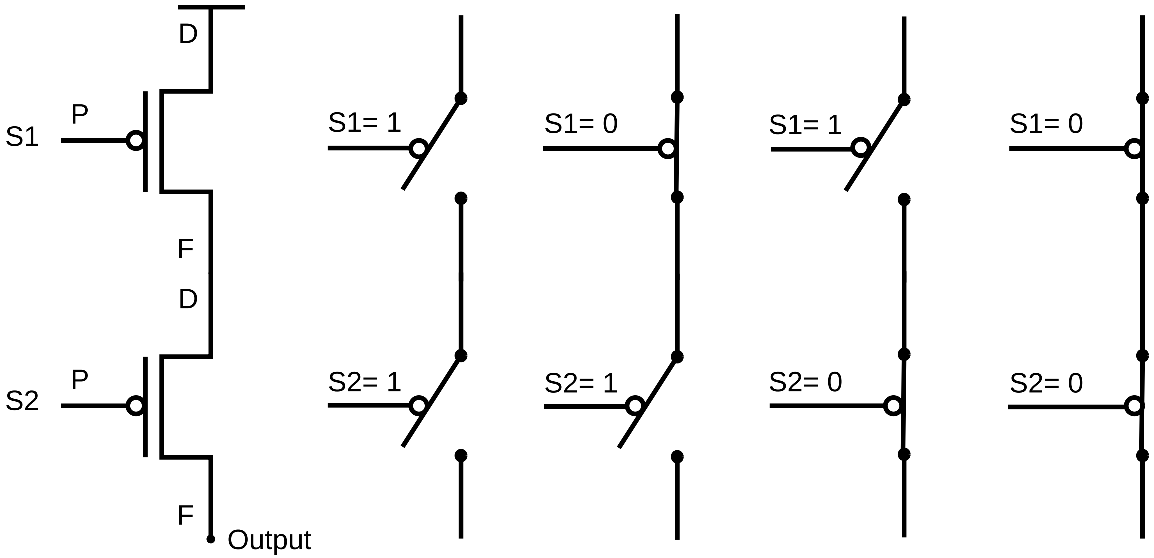
MOS Technology

- Series nMOS transistors:
  - – Output = 0 *if* S1=1 *and* S2=1



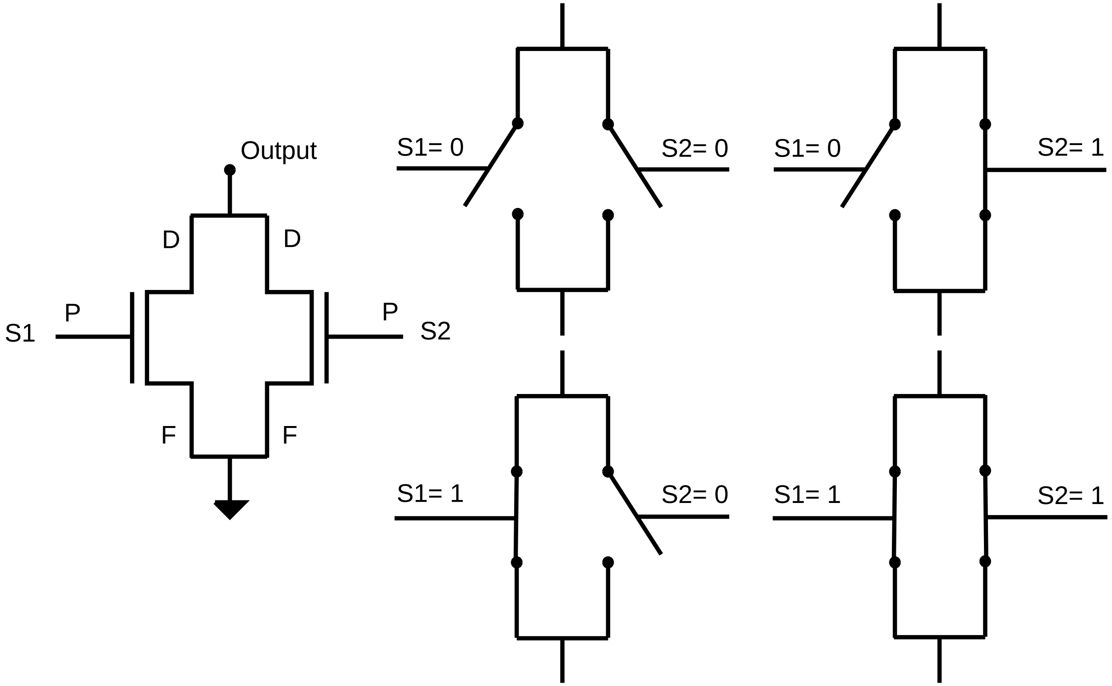
MOS Technology

- Series nMOS transistors:
  - Output = 1 *if* S1=0 *and* S2=0



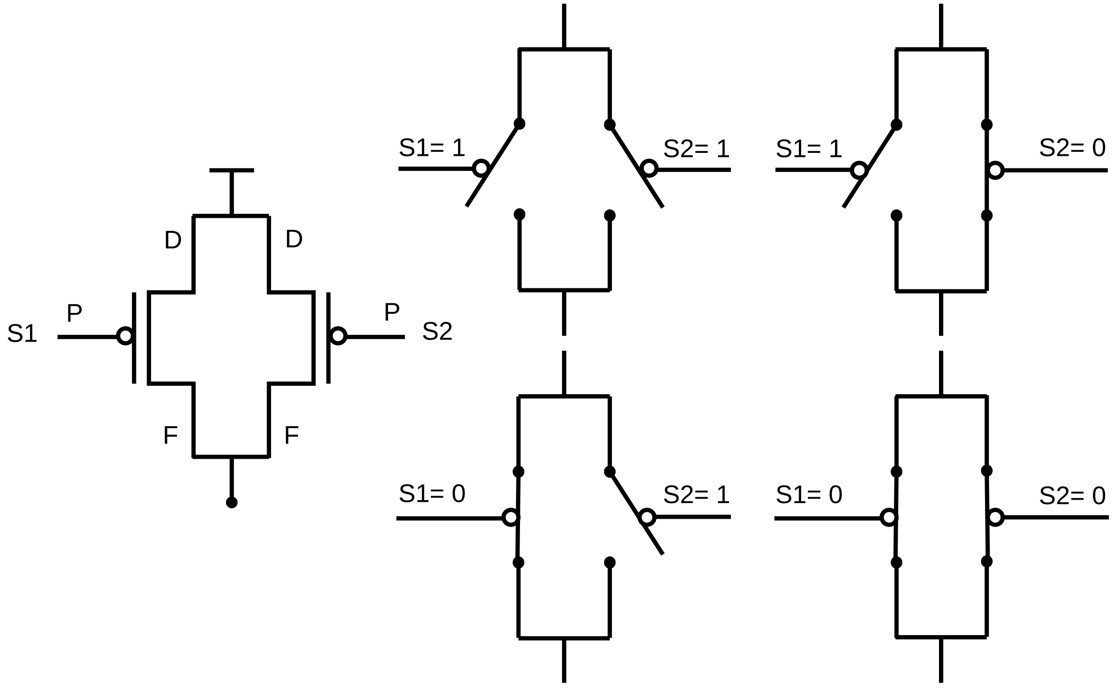
MOS Technology

- Paral·lel nMOS transistors:
  - Output = 0 *if* S1=1 *or* S2=1



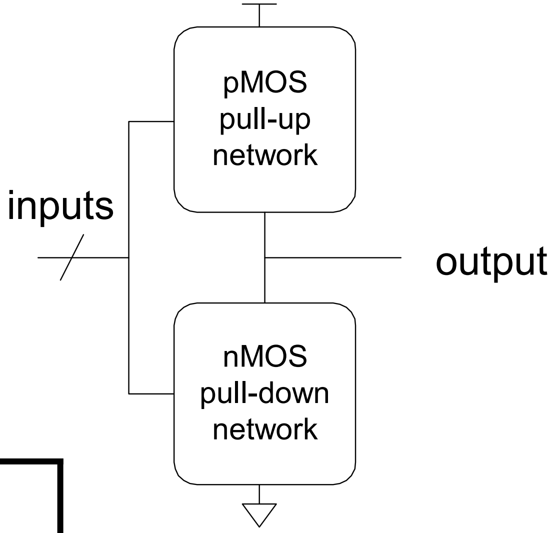
MOS Technology

- Paral·lel nMOS transistors:
  - Output = 1 *if* S1=0 *or* S2=0



Complementary CMOS

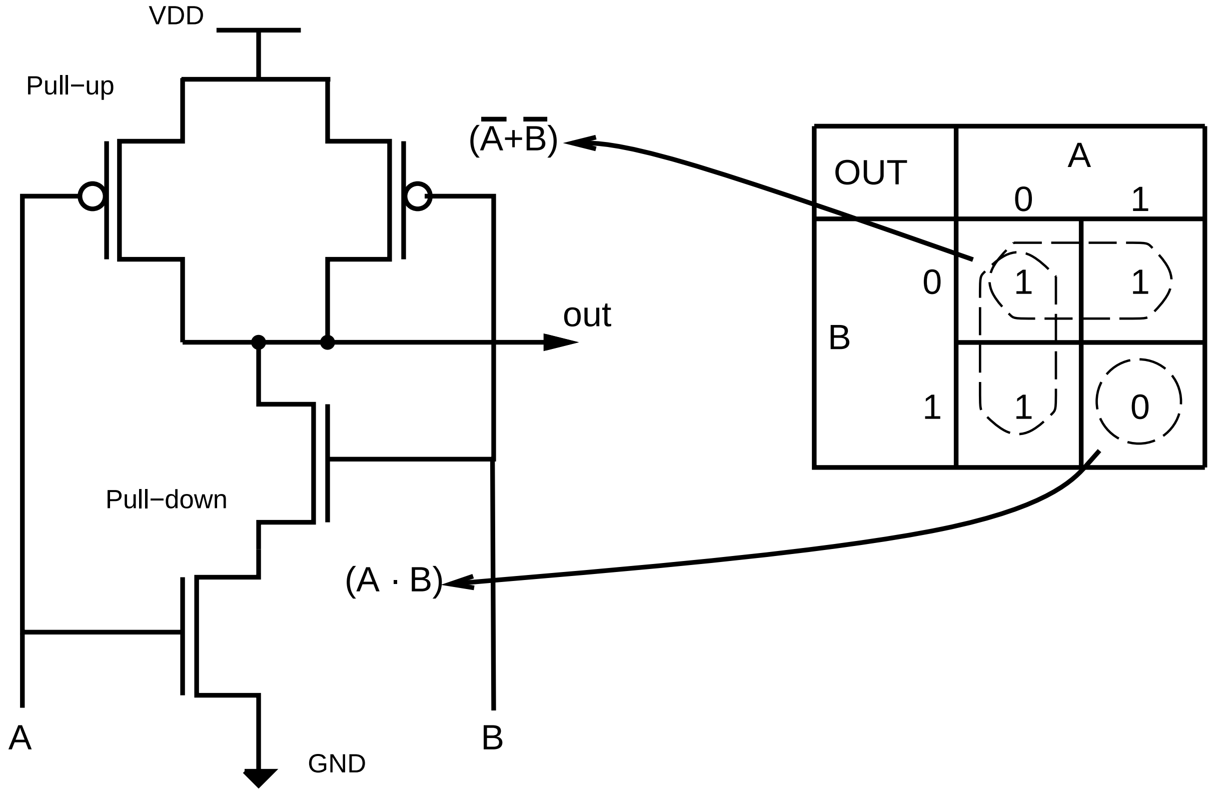
- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

CMOS Gates

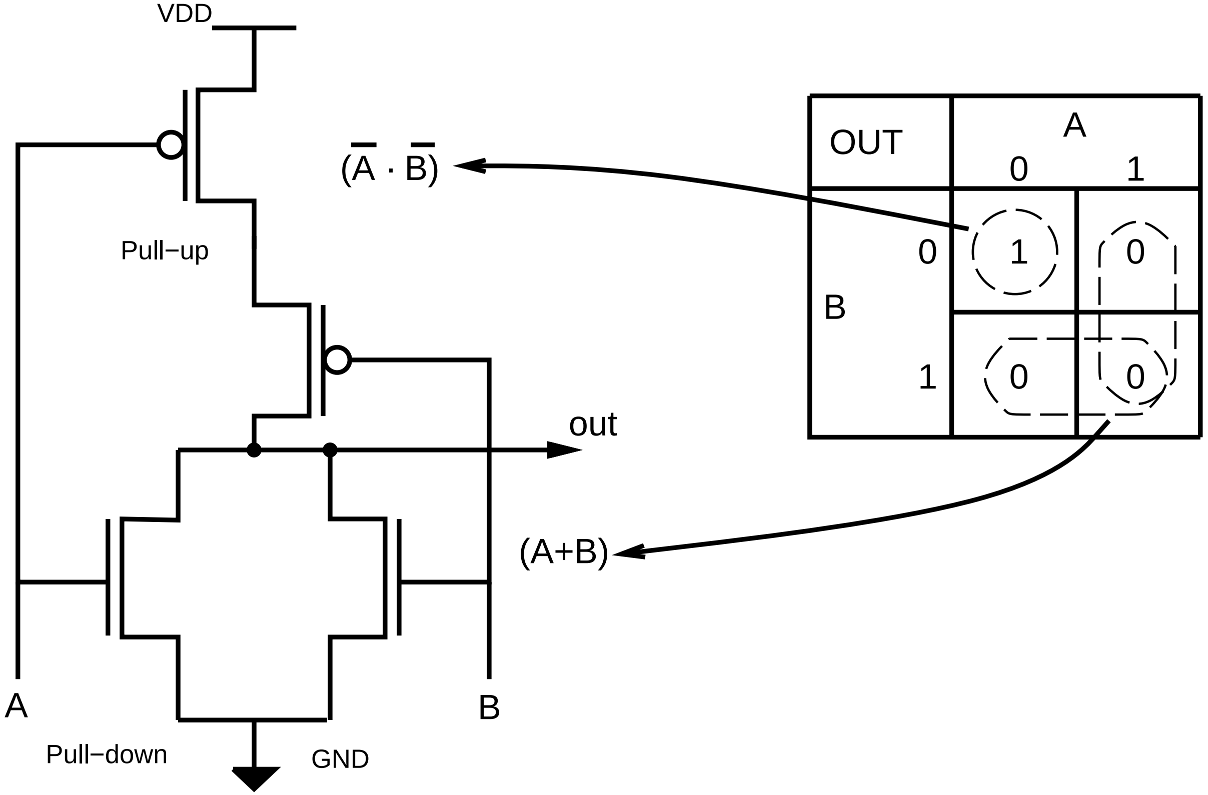
- NAND



OUT		A	
		0	1
B	0	1	1
	1	1	0

CMOS Gates

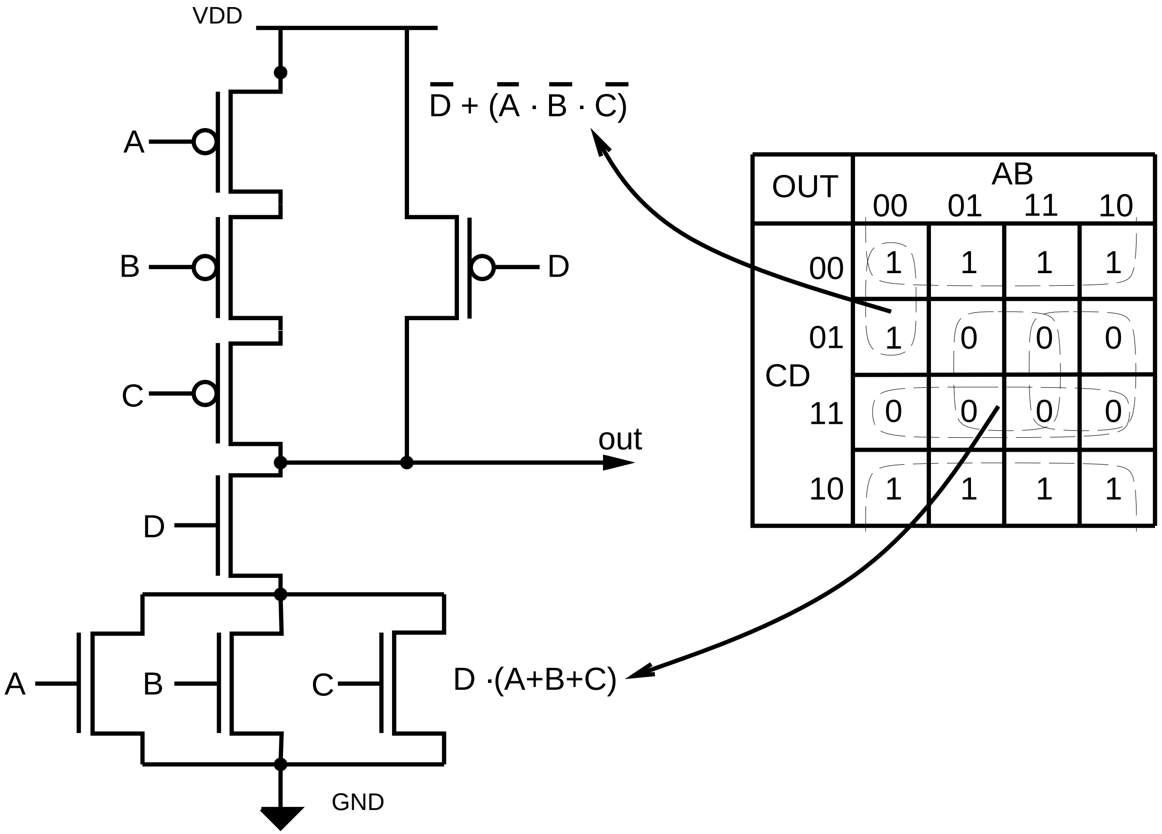
- NOR



OUT		A = 0	A = 1
B	0	1	0
	1	0	0

CMOS Gates

- Complex gates

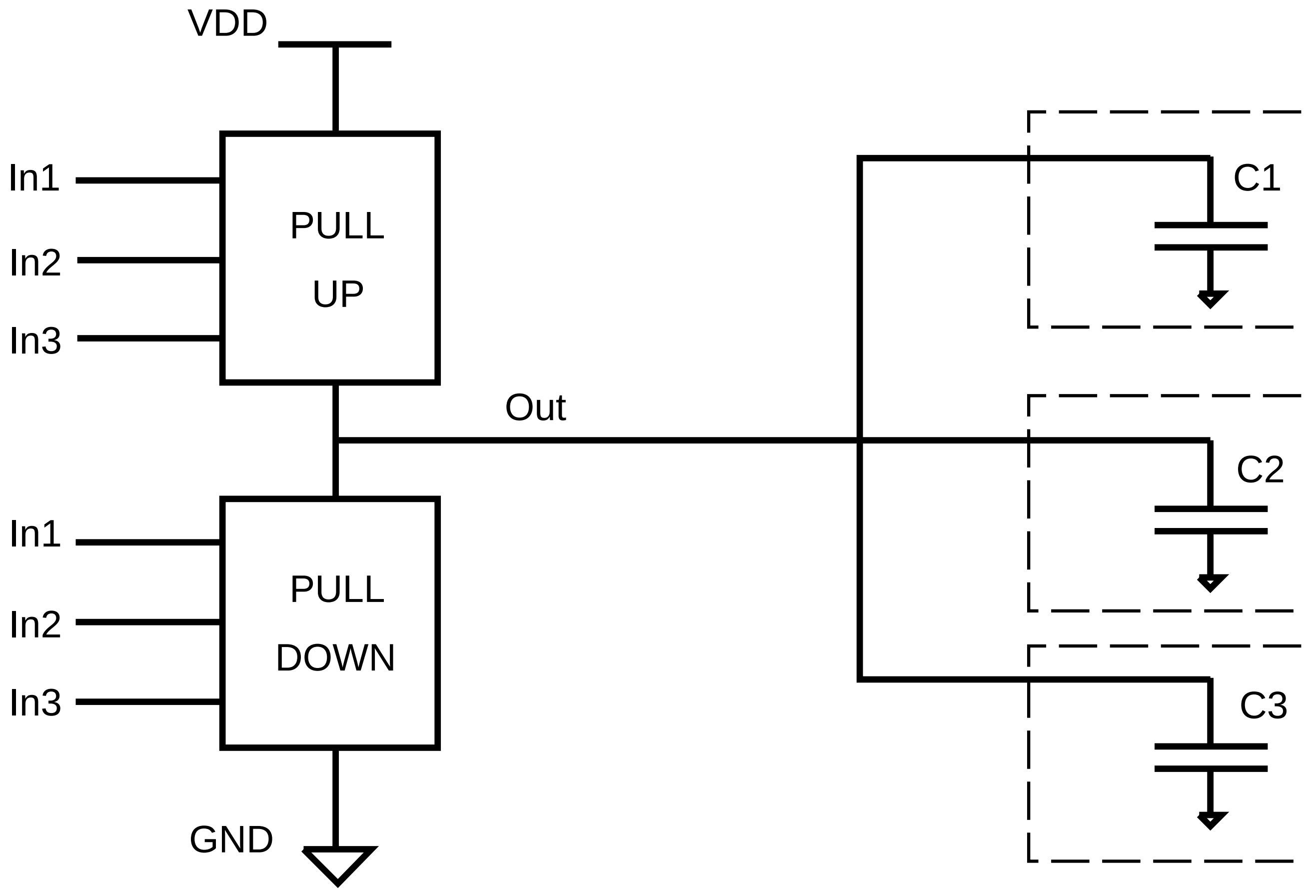


OUT	AB 00	01	11	10
CD 00	1	1	1	1
01	1	0	0	0
11	0	0	0	0
10	1	1	1	1

CMOS Gates

- Design of inverted functions :
  - F= !(……)
  - AND "·":
    - Pull-down: Transistors nMOS in series
    - Pull-up: Transistors pMOS in parallel
  - OR "+":
    - Pull-down: Transistors nMOS in parallel
    - Pull-up: Transistors pMOS in series

General CMOS structure:



MOS transistor resistance

- An approximation to the drive current ability.

- The resistance is:
  - Directly proportional to the channel Length (L).
  - Inversely proportional to the transistor width (W).

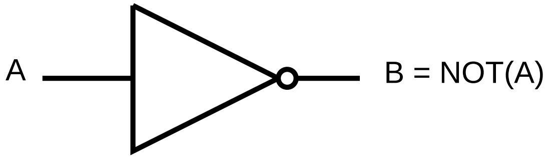
  - R~L/W

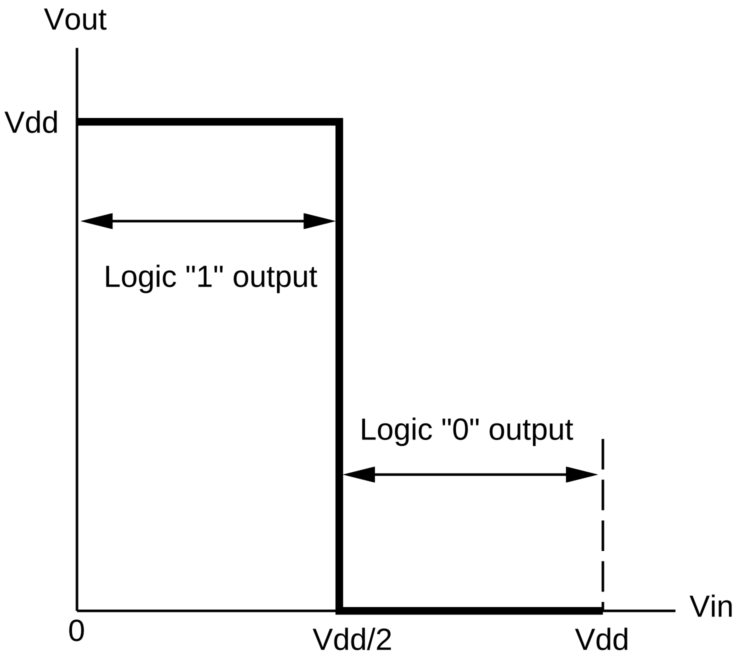
- In bulk CMOS, pmos transistors have double the resistance of the nmos.

$$R_{sp} \approx 2 R^{s}$$

- Transistor sizes can be defined as:
- Real values (in lambdas or nm)
- The ratio (i.e. Form factor) against the minimum sized (2λ)

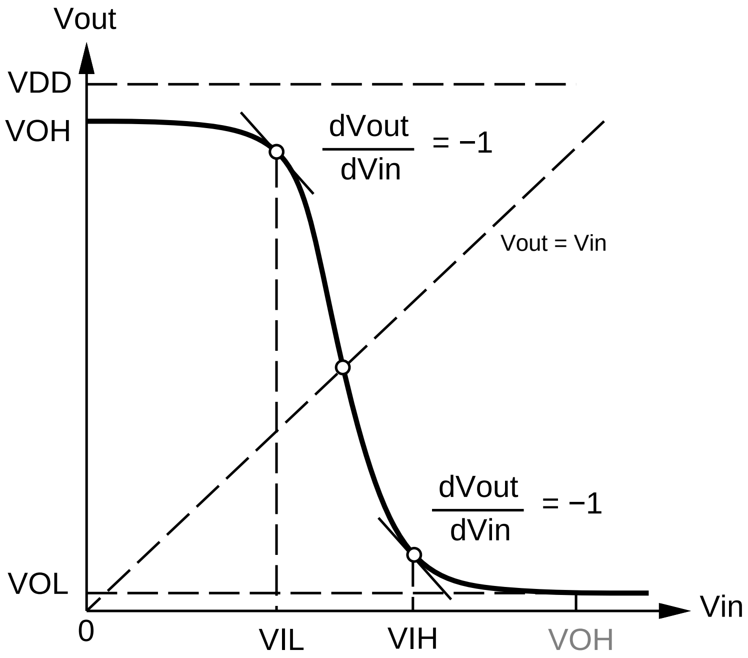
Ideal Voltage Transfer Curve

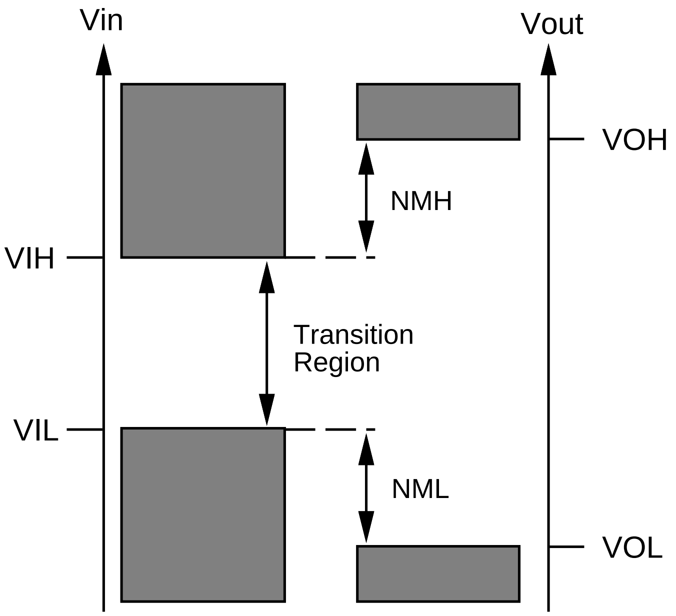


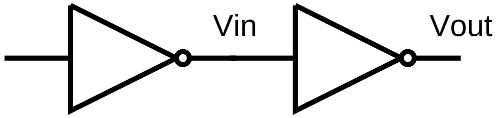


- The real curve is much more complex. It depends on the resistance and capacitances of all the materials/layers involved.

Real Voltage Transfer Curve



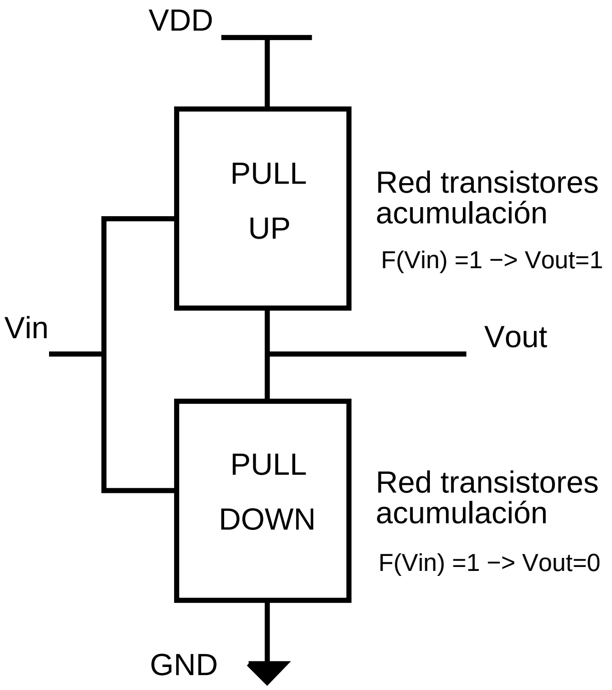




- The transfer curve determines the noise margins (NM) and the region of uncertainty.

CMOS Inverter

- Function implemented in the pull-up and the pull-down
- Small static power when compared to previous technologies (i.e. Nmos, bipolar)

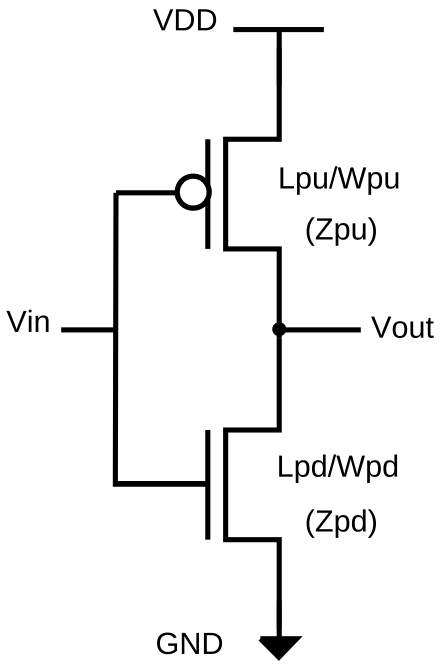


Red transistores acumulación

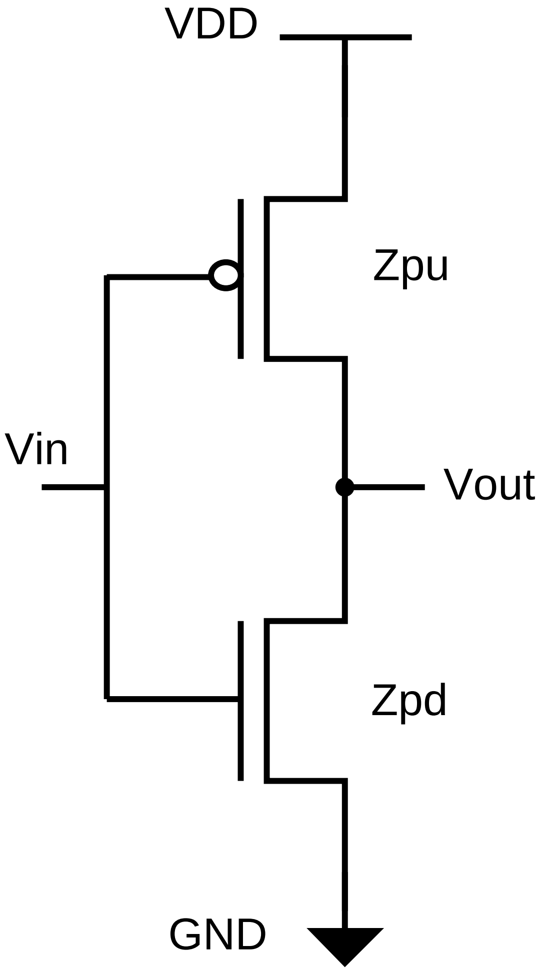
F(Vin) =1 -> Vout=1

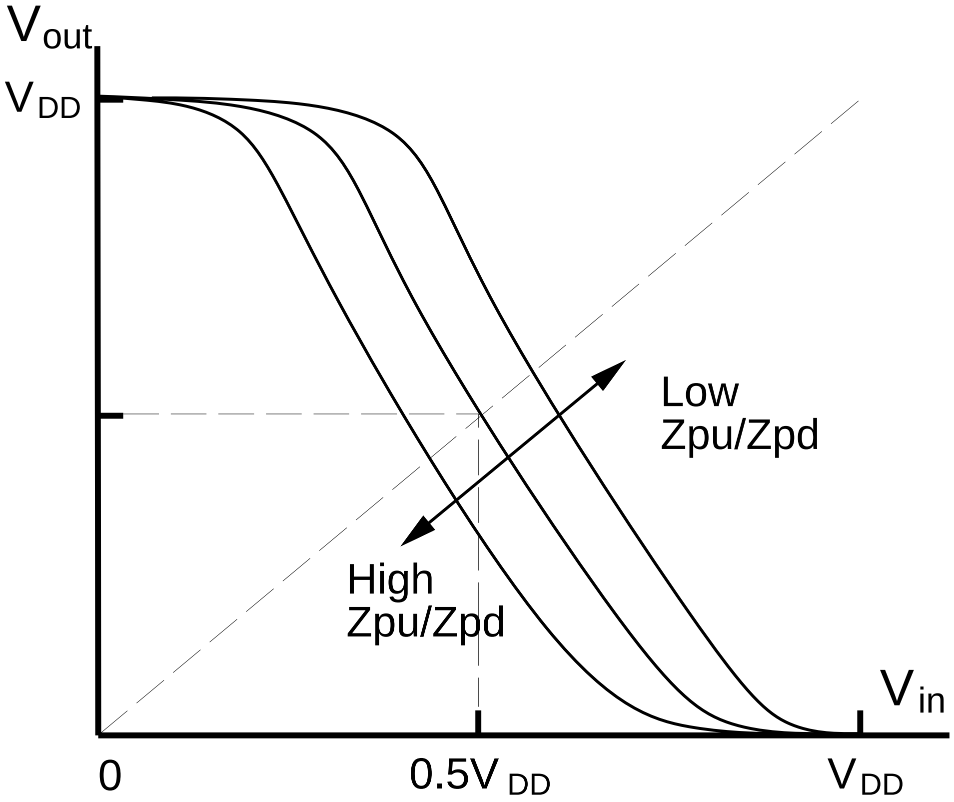
Red transistores acumulación

F(Vin) =1 -> Vout=0



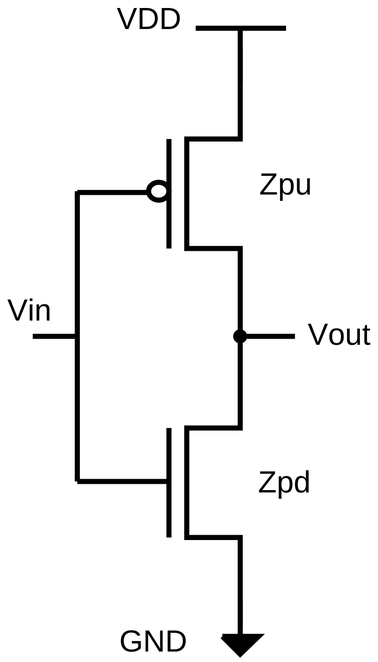
CMOS Inverter

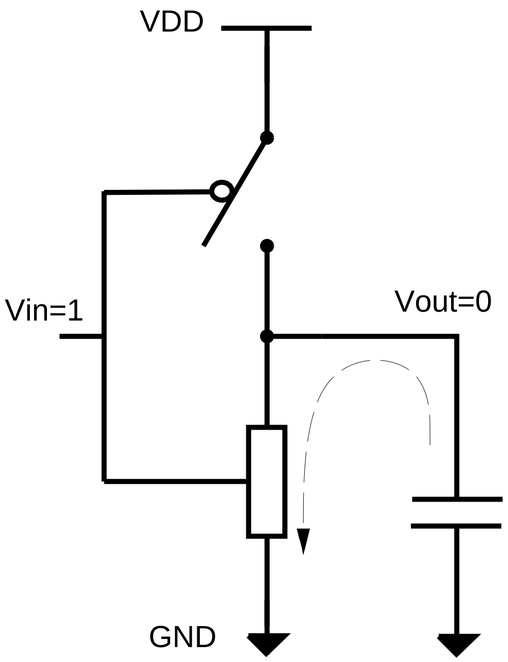


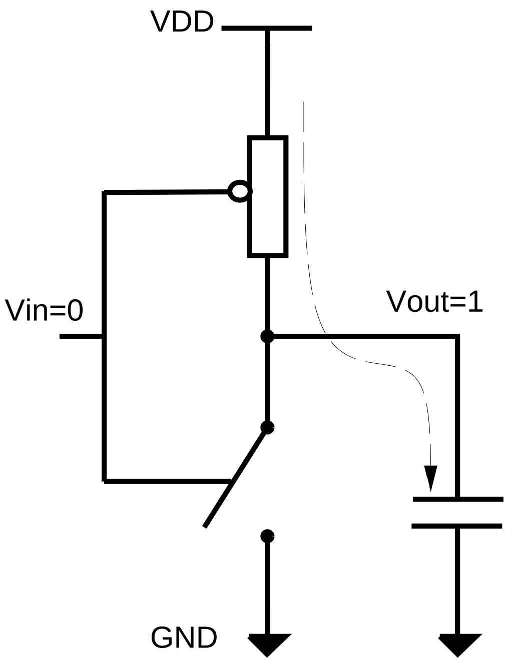


Inversor CMOS

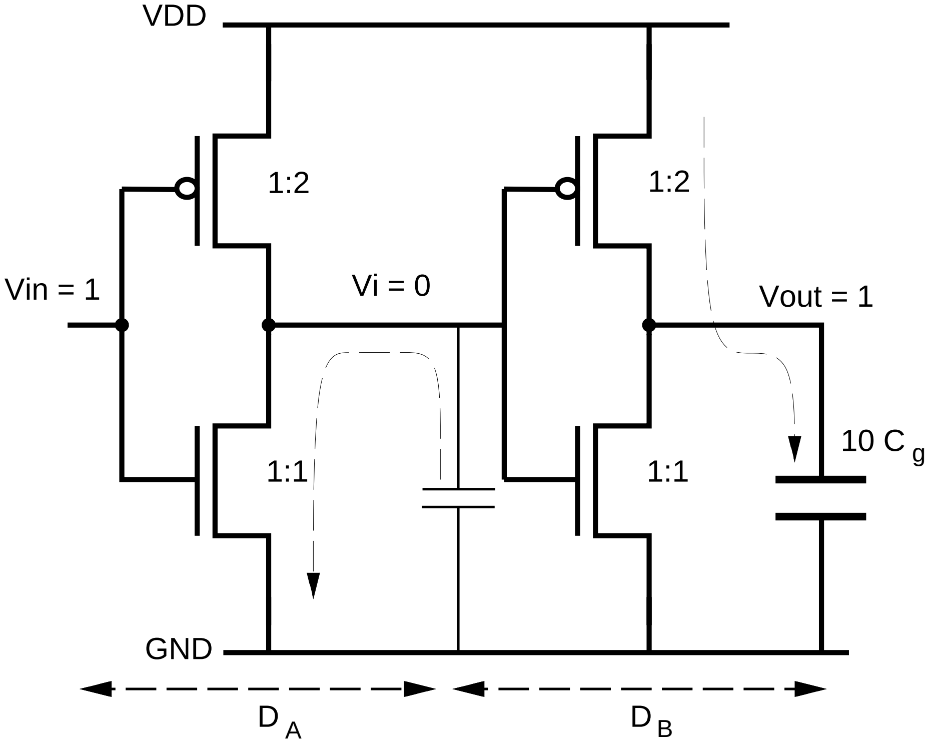
- Simetrical delays if R_{pu}=R_{pd} (given 1R_{sp} = 2R_s)





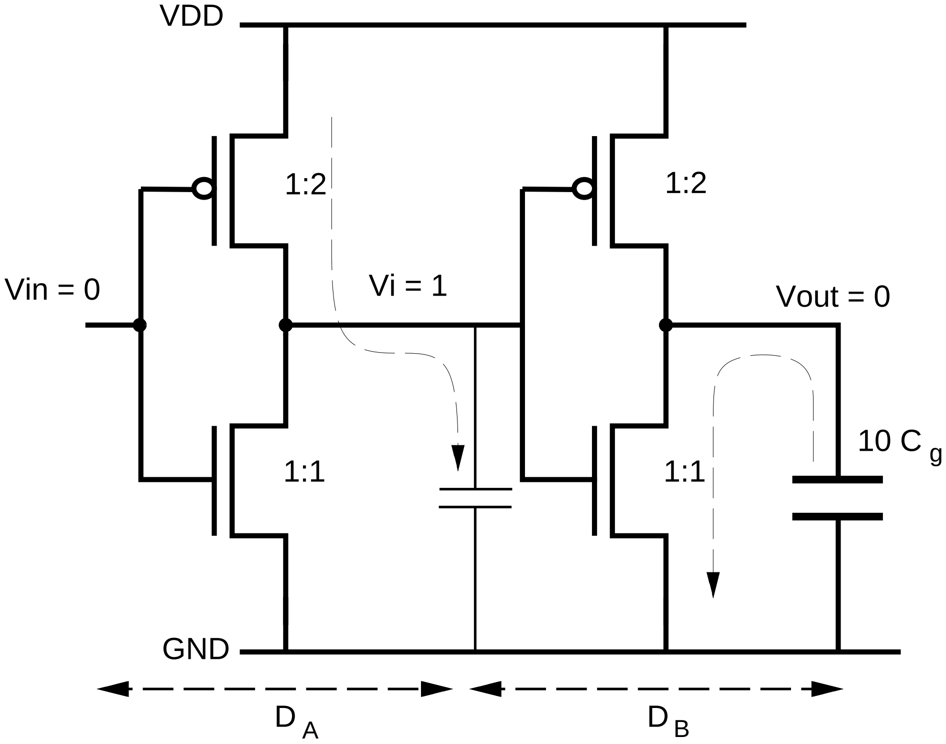


CMOS Inverter Delays



$$C_i = \frac{2\lambda \cdot 4\lambda}{2\lambda \cdot 2\lambda} C_g + \frac{2\lambda \cdot 2\lambda}{2\lambda \cdot 2\lambda} C_g = 3C_g$$

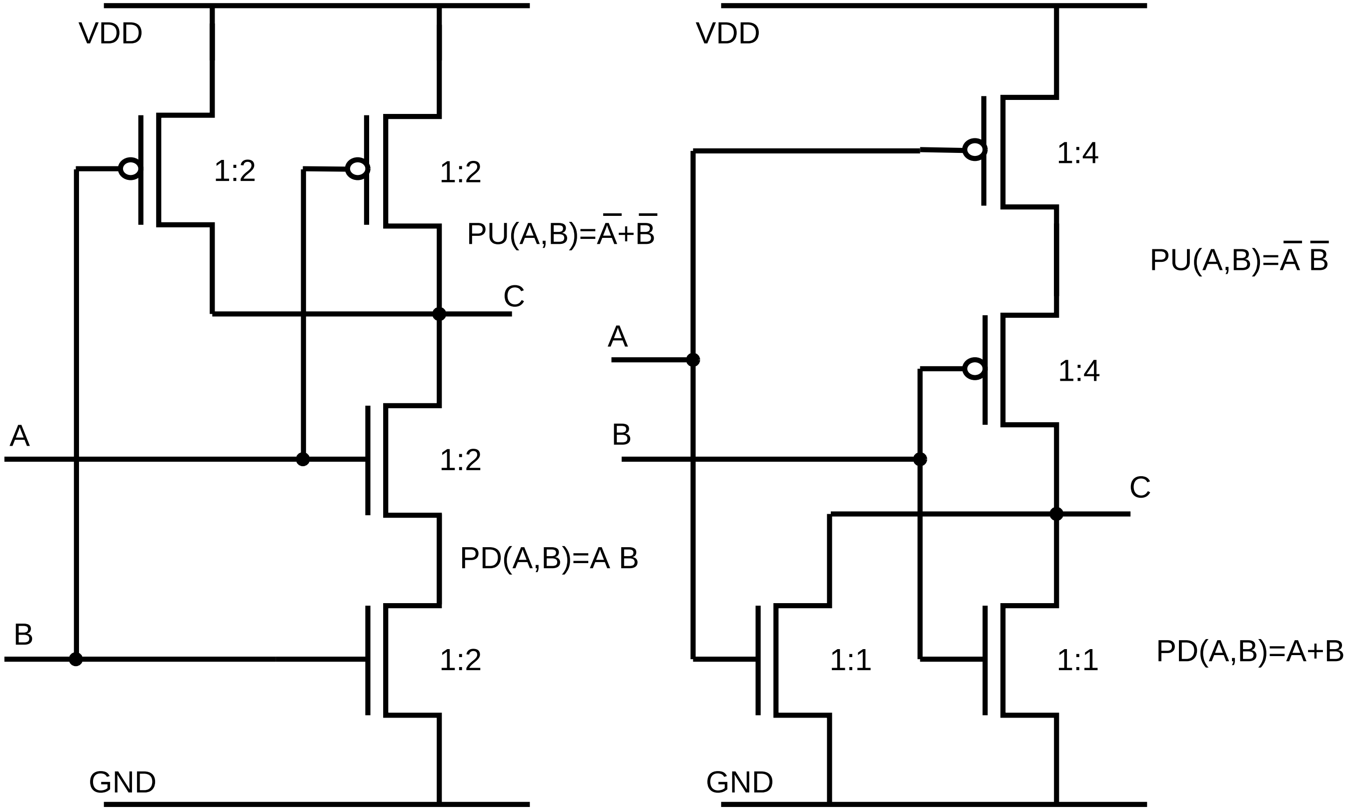
$$\tau_{1-1} = \frac{2\lambda}{2\lambda} R_s \cdot 3C_g + \frac{2\lambda}{4\lambda} R_{sp} \cdot 10C_g = 13\tau$$



$$1R_{sp} = 2R_s$$

$$\tau_{0-0} = \frac{2\lambda}{4\lambda} R_{sp} \cdot 3C_g + \frac{2\lambda}{2\lambda} R_s \cdot 10C_g = 13\tau$$

Other CMOS gates



NAND NOR

Case study

Standard Cell implementation

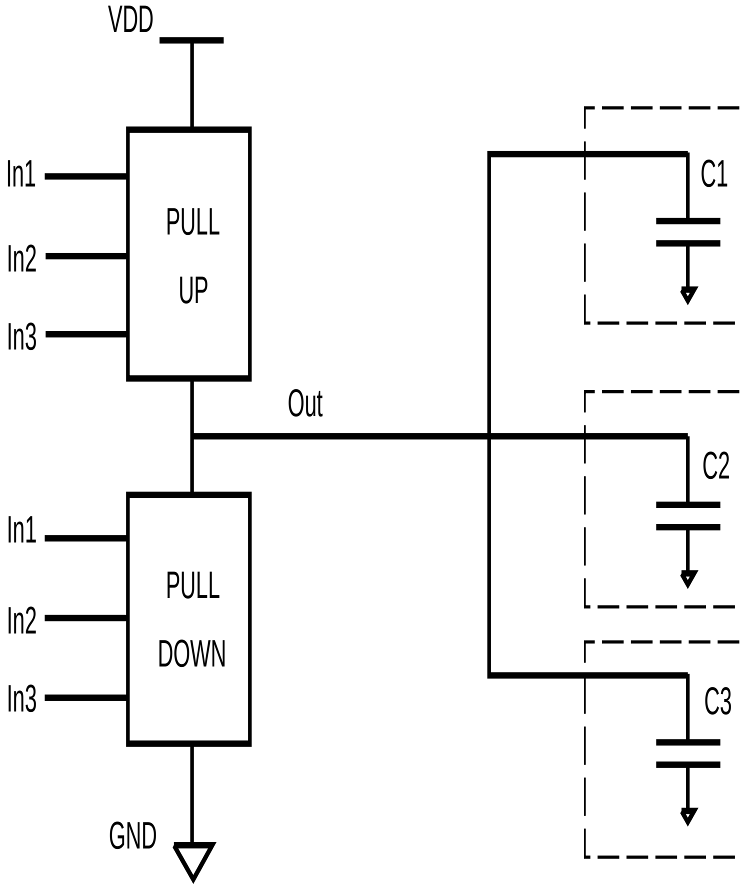
Standard Cell Implementation

- Cells designed in a certain pattern
- Due to the *standard* pattern they can be used in several circuits

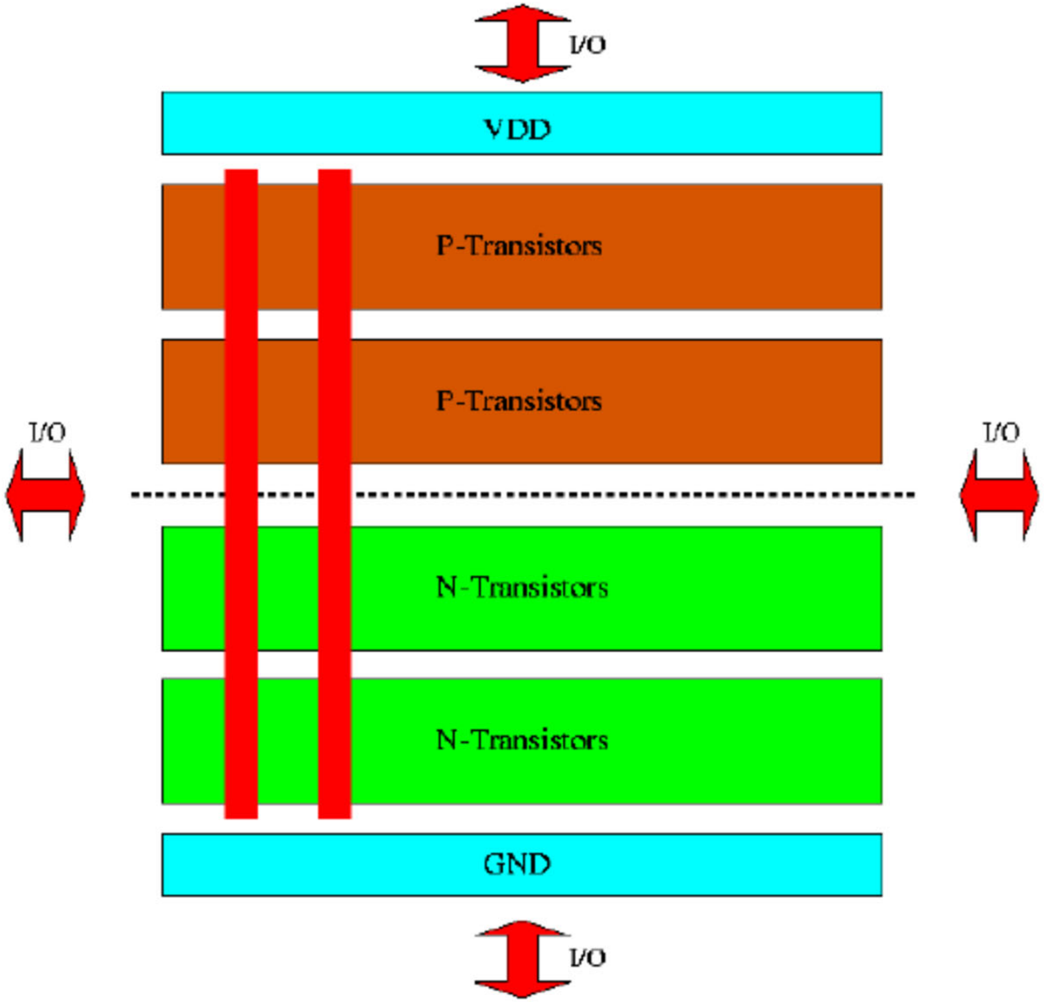
\+ Design reuse

\- Non-adaptative design

A typical MOS gate



Standard Cell Structure



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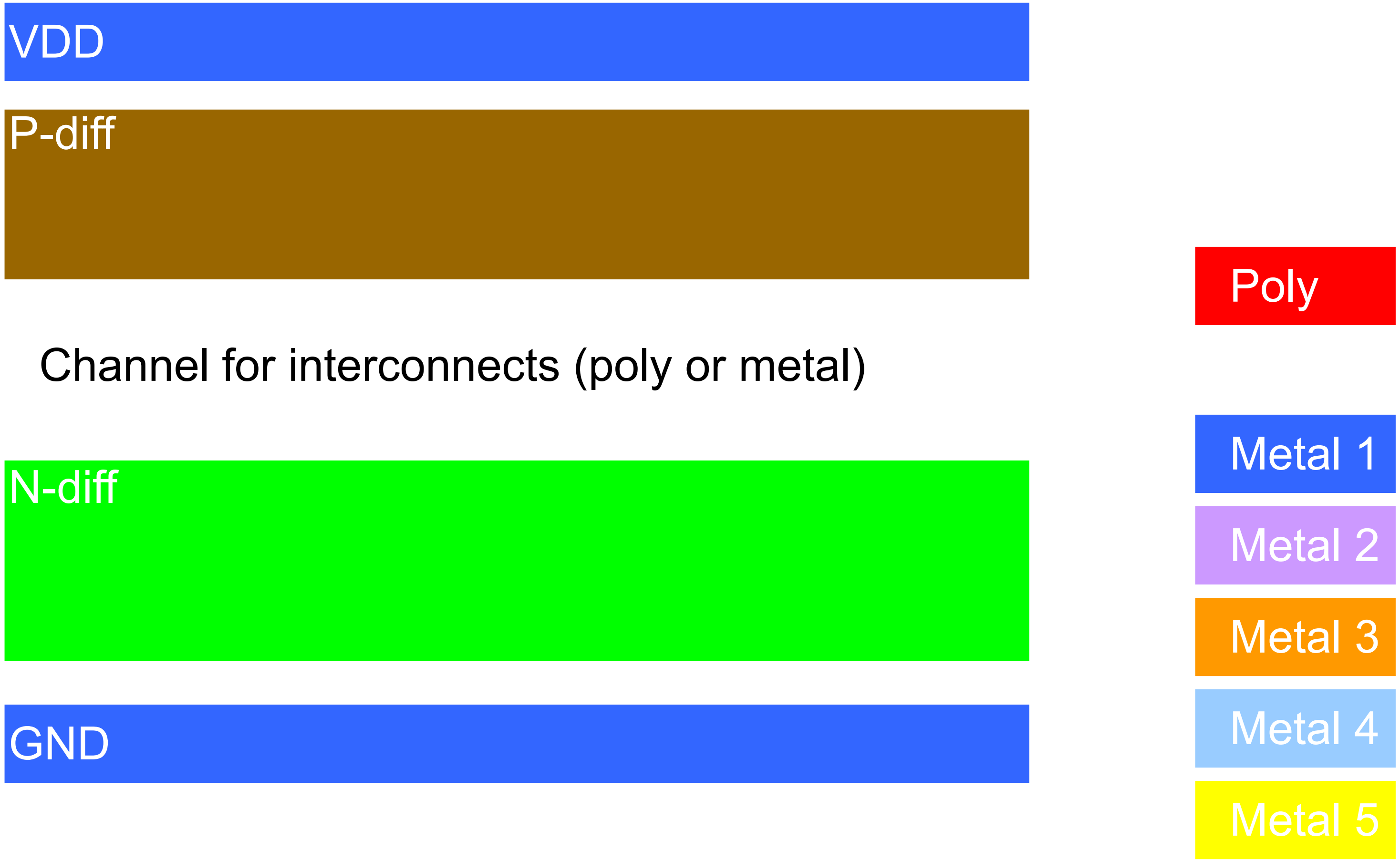


VDD

P-diff

Channel for interconnects (poly or metal)

N-diff

GND

Poly

Metal 1

Metal 2

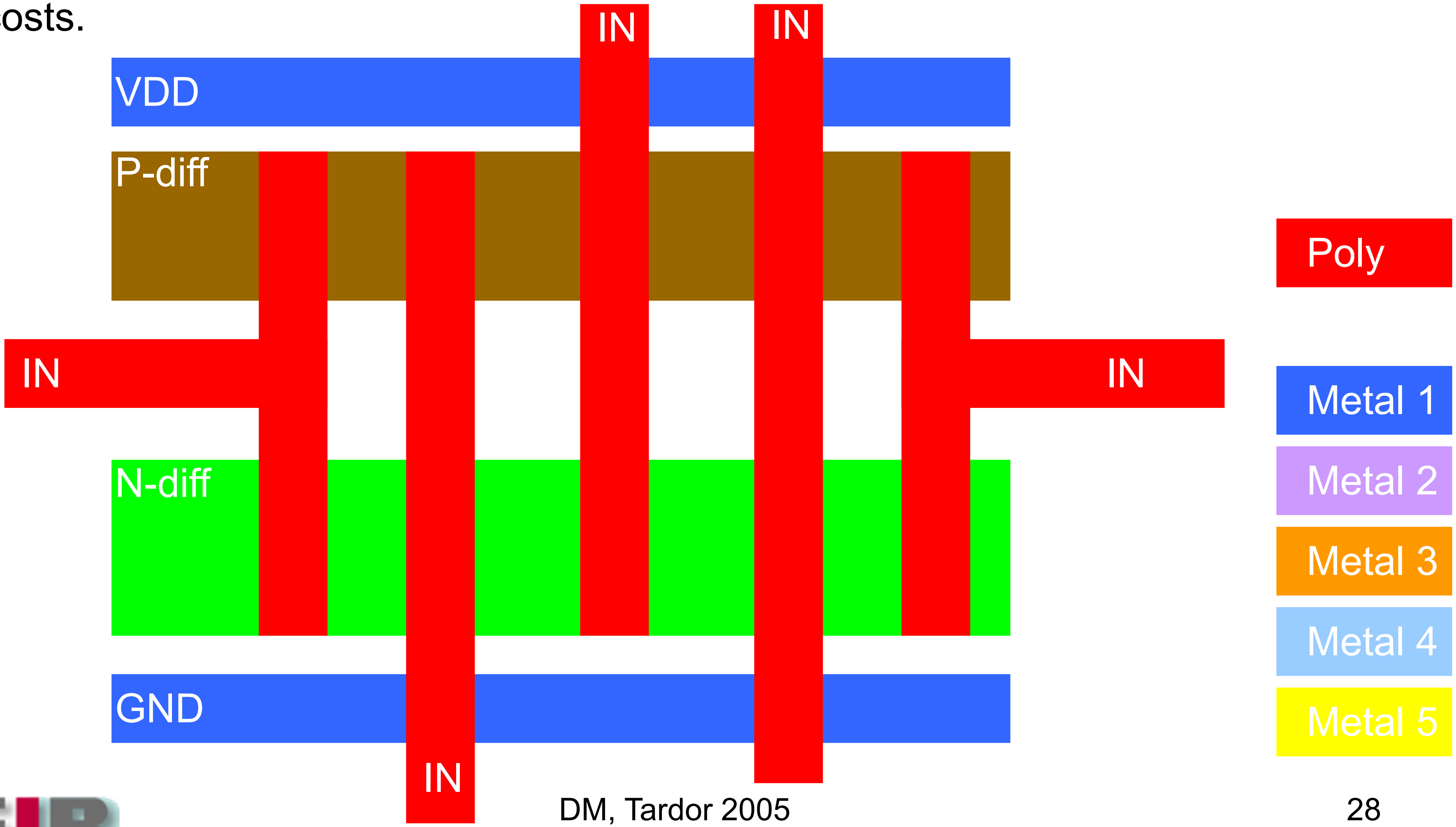
Metal 3

Metal 4

Metal 5

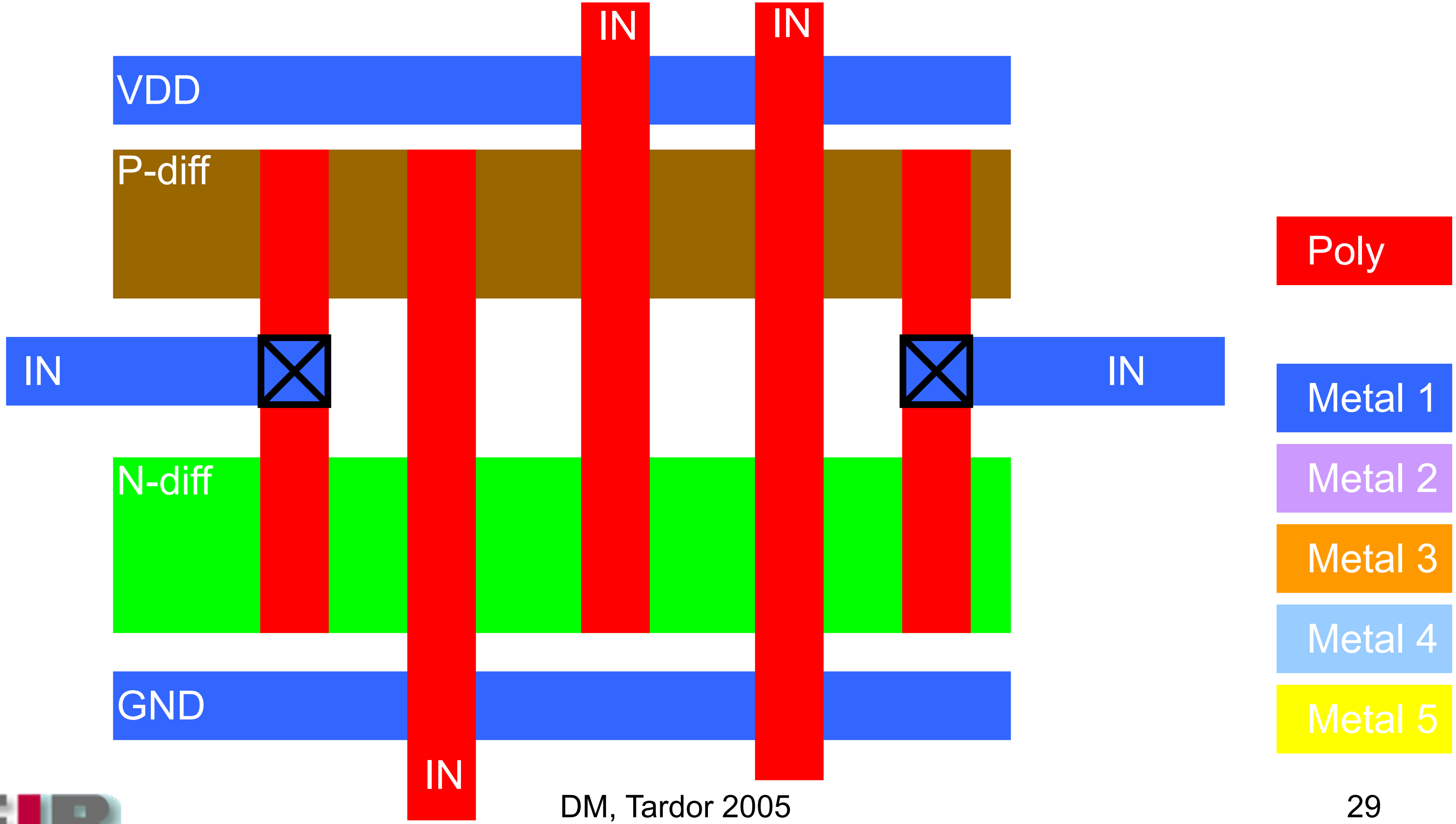
Standard Cell Structure

The inputs of the transistors are connected to the poly layer. Horizontal connections are not recommendable since they increase the manufacturing costs.



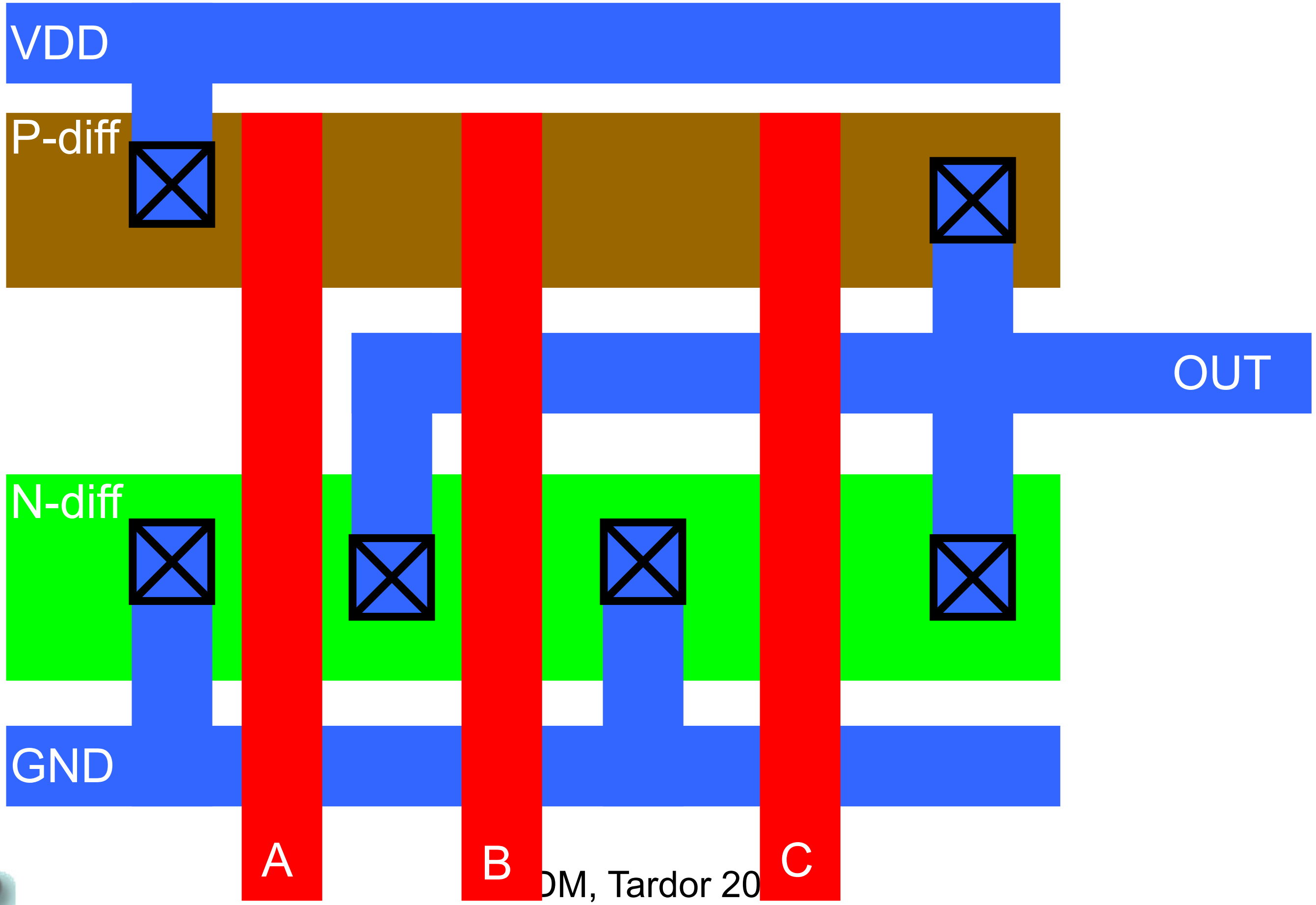
Standard Cell Structure

The inputs of the transistors are connected to poly or to metal –in case they are lateral inputs.



Standard Cell Structure

Transistors are placed in a serial way. If we want them in paral·lel we will have to add metal connections.



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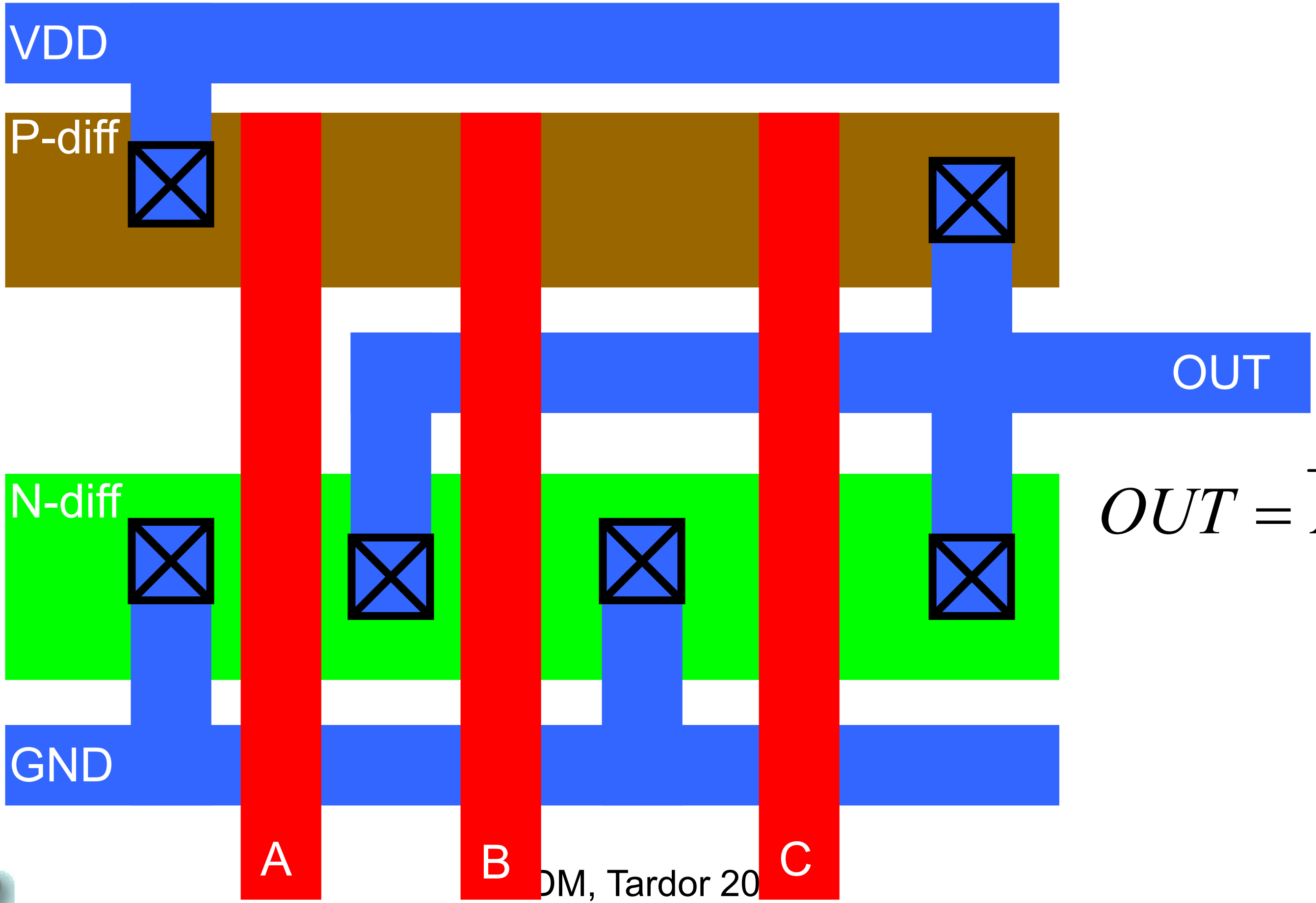

$$OUT = \overline{A + B + C}$$

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