Nanoelectronic Circuit Design

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Master MIRI

Q2 2018/2019

Departament d'Arquitectura de Computadors

UNIVERSITAT POLITÈCNICA DE CATALUNYA

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Professor

Ramon Canal

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- Office hours:
  - Tue 11-13h, Thu. 15-17

    (check in before you come)

Course info and docs

http://docencia.ac.upc.edu/master/MIRI/NCD/

- Course information
  - Notes and slides
  - Assignments
  - Lab sessions and documentation

Agenda

- Course structure
- Evaluation
- What will I be able to do after the course?
- Topics covered
- Lab sessions
- Course Schedule
- Bibliography

Course structure

- Lectures
  - Monday 8h-10h
  - Wednesday 8h-10h
- Assignments
  - Problem sets (first 3 weeks)
  - Lab sessions (next 9 weeks)
  - Final project (last 3 weeks)

Evaluation

- Final mark will be based on the performance of:
  - Course work
  - Lab sessions
  - Final project
  - Elevator pitch

Topics Covered

0. Historical Perspective
1. Introduction to MOS and VLSI Technology
2. Advanced MOS Design
   a. VHDL Description
   b. Area, Delay and Power Modeling
3. VLSI Design
   a. VLSI Design Stages
   b. Placement Techniques
   c. Routing Techniques
4. Thermal and Energy Analysis of Microprocessors
   a. Memory Structures
   b. Interconnect Structures
   c. System Level Modeling

Topics Covered

5. Design Implications of Temperature and Power
    a. Compile-time Techniques
    b. Run-time Techniques
6. Design for Reliability
    a. Inter-Die variation
    b. Intra-Die variation
    c. Transient errors and permanent faults
7. Technology outlook
    a. Future and emerging technologies

Lab sessions

- SPICE design

  Compulsory:

  – Introduction, gate design (lab 1)
  – Memory Design (lab 2)
  – Power Measurement (lab 3)
  – Variability Introduction (lab 4)

  Optional – equivalent to final project:

  – Cache evolution through technology (lab 5)
    - Area, Delay, Power and robustness analysis of a cache across different technology nodes.

Assignment/Lab schedule

Name	Due Date
Historical Perspective	18/02/2018
Logic Gate Design with CMOS	24/02/2018
Logic Gate Implementation	4/03/2018
Lab Session 1	18/03/2018
Lab Session 2	1/04/2018
Lab Session 3	29/04/2017
Lab Session 4	20/05/2017

Final Project

FINAL PROJECT (One of those)	
1.CACTI extensions with NVM cells	
2.Lab session 5	
3.Presentation of one recent paper	
Your choice must be emailed by :	**13/05/2018**
Presentations will start :	**27/05/2018**
Presentations will end :	**29/05/2018**
Other projects will be handled in by :	**21/06/2018**

The course has two marks:
1) Final Project + Elevator Pitch (E)
2) The assignments + lab sessions (Lab)

The final mark will be computed as: 0,4 x Lab + 0,6 x E

Bibliography

- CMOS VLSI Design : A Circuits and Systems Perspective (3rd Edition), Neil H.E. Weste, David Harris, Addison Wesley, 2004
- Design Variability (Synthesis Lectures on Computer Architecture), David Brooks, Morgan & Claypool, 2013
- Fault Tolerant Computer Architecture (Synthesis Lectures on Computer Architecture), Daniel J. Sorin , Morgan & Claypool, 2009
- Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic; Digital Integrated Circuits: A Design Perspective; Editorial Prentice Hall, 2003

Other interesting videos

- Silicon Valley: The untold story (2018, Science channel, miniseries)
- Podfather - Robert Noyce and the Rise of Silicon Valley (2009, BBC)