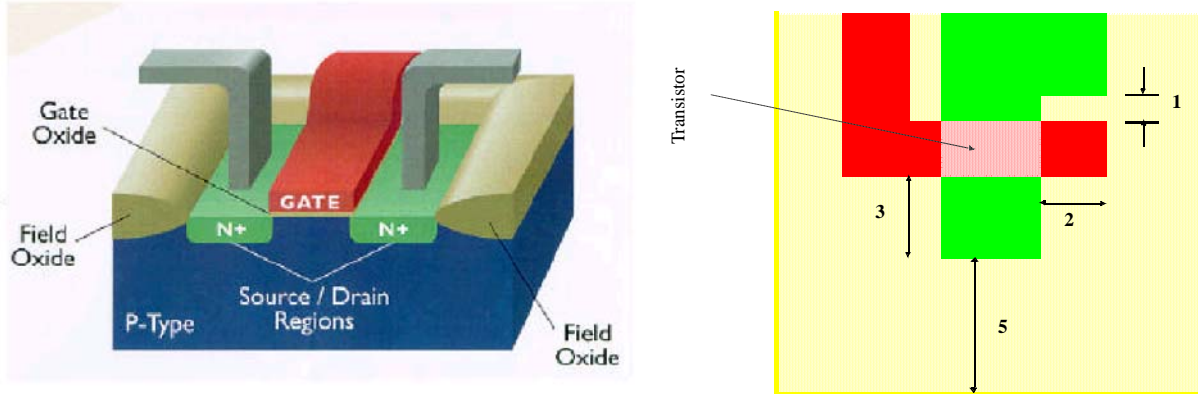


CMOS basic concepts II

In this document we will see how transistors are implemented. Once we know the implementation details we will then be able to build any circuit we want since the notation will stay –for ever- the same.

This is a picture of a transistor 3-D (left) and 2-D (right)



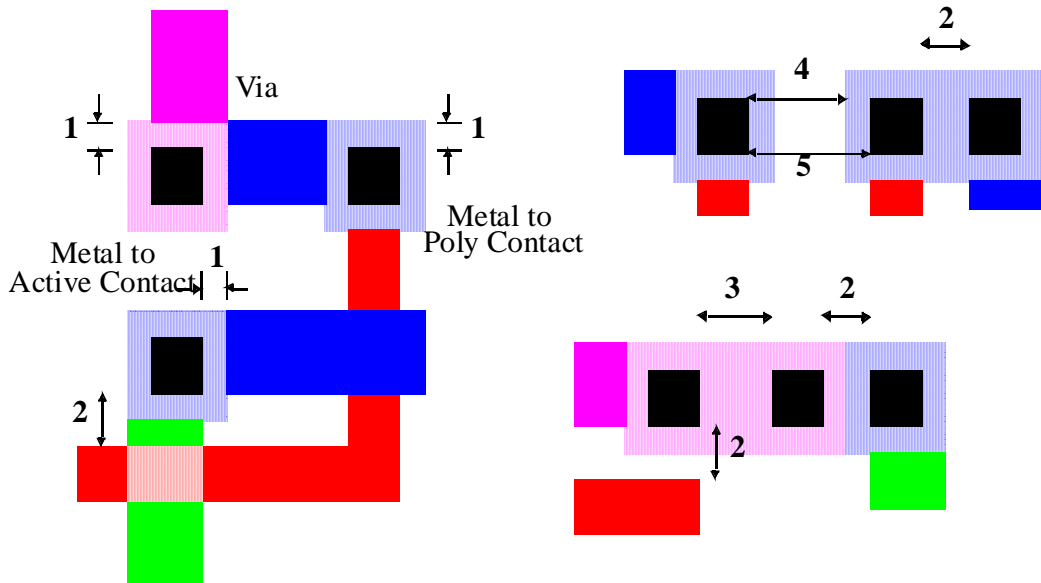
The *gate* is implemented in polysilicon (and it will be the red stripe). When the polysilicon crosses an N-type diffusion (green) then it creates an NMOS transistor. In the same way, when the polysilicon crosses a P-type diffusion (usually brown) then we have a PMOS transistor.

Apart from these materials, it is also feasible to connect terminals using the available metal layers. These are identified by blue (first metal layer), lila/violet (second level), etc. In our designs, it is enough to use 2 metal levels.

To connect the different levels/materials we will use *contacts*. For every material-level pair we will use a different contact type (they are usually labeled with the corresponding materials/levels. I.e. ndif-metal1 contact). Sometimes, the contacts between metal levels are called *vias*. The full color scheme for a 250nm technology is the following:

Layer Description	Representation				
metal					
	m1	m2	m3	m4	m5
well					
	nw				
polysilicon					
	poly				
contacts & vias					
	ct	v12,v23,v34,v45	nwc	pwc	
active area and FETs					
	ndif	pdif	nfet	pfet	
select					
	nplus	pplus	prb		

In the figure, there are more material/types than have been explained so far but we will not make use of them. In the next figure, the different contacts between levels and materials are shown:



Due to the imprecision when manufacturing, some minimal distances among objects are recommended. These distances are the numbers in the figure above. When designing any circuit it is important to keep these distances. Actually, the CAD tools incorporate these restrictions so the user is always aware of them. These restrictions are often called *Design Rules*.

Once we know how we draw transistors at a low level, we can start implementing a circuit. (see Lab sessions in the webpage).

- Draw the *layout* for the following functions:

- $Z = \overline{A + B + C + D}$
- $Z = \overline{((A \cdot B \cdot C) + D)}$