

HP EXTENDS PA-RISC WITH 8700

By Kevin Krewell {5/22/00-02}

HP plans to update its PA-RISC offering in 2001 with the PA-8700, which will have larger caches and higher frequencies than the 8600 it ships today. Shipments of the 8700 are expected to begin in the first half of 2001. HP is projecting a minimum clock speed of

800MHz, which is not terribly impressive considering that Intel should have Willamette-based Foster processors running at twice that speed by then. HP, however, believes that next year the 8700 will deliver performance competitive with that of other 64-bit server processors, such as Intel's Itanium, Sun's UltraSPARC III, and IBM's I-Star. HP continues to enhance the PA-RISC line, even though it has invested heavily in the IA-64 architecture, as it cannot afford to wait until its existing customer base accepts the IA-64 architecture. In the meantime, HP will use advanced process technology to move PA-RISC processors forward.

Initially, the 8700 should be competitive with the first IA-64 processor, Itanium, and, for a time, HP's PA-RISC will compete with customers of Intel, its partner in IA-64 development. Eventually, HP will offer both architectures in the 64-bit server market, at which time it will also compete with itself. The benefit of this dual-architecture strategy is that it allows PA-RISC customers to migrate gradually to IA-64. HP's roadmap shows PA-RISC coexisting with IA-64, at least until 2002. Future PA-RISC offerings will include the PA-8700, 8800, and 8900. The roadmap also shows that IA-64 will have a steeper performance ramp than PA-RISC, with the IA-64 pulling ahead in 2002, based on the strength of the Deerfield and Madison processors. After 2002, PA-RISC disappears from HP's roadmap.

An extraordinarily large on-chip L1 cache has characterized each member of the 8x00 family since the 8500. The 8700 continues in this vein, pushing the limits with 2.25MB of on-chip L1 cache. This amount of cache was made possible

by HP's foundry partner for the 8700, which is capable of supplying a 0.18-micron seven-layer-copper silicon-on-insulator (SOI) process. These are process features that only one foundry is expected to offer in early 2001—IBM Microelectronics.

A significant amount of redesign was required to transfer the 8600 core to the new process. The 8700 benefits from process improvements by having the on-chip memory increased while the area used by memory remains at about 52%. That has been made possible by the 0.18-micron process used to create a new SRAM cell that is only 37% of the size of the 8600's 0.25-micron SRAM cell. The copper SOI process will also allow the 8700 to reach higher clock speeds, jumping from 550MHz to at least 800MHz, while keeping power dissipation to a reasonable level.

The expanded L1 caches and higher clock frequency will provide the bulk of the performance increase over the 8600. The 8700, with 1.5M of data cache and 750K of instruction cache, has 50% more cache than the 8600, which has 1M of data cache and 500K of instruction cache). The larger L1 caches should help the 8700 remain competitive on server benchmarks such as SPEC and TPC-C.

But extremely large on-chip caches have a downside—they create some huge die sizes. The 8600, for example, has a die size of 477mm², which surely must be a challenge to manufacture. Because of the new process, however, the 8700 will have a die size of only 304mm², still a large die but one that is significantly smaller than that of its predecessor. To further improve manufacturing yields, the 8700 will add more redundancy to the SRAM arrays.

HP provides good data security, with single-bit error correction on the data cache and parity checking on the instruction cache. Parity checking was deemed sufficient for the instruction cache because it is less sensitive to read-write errors, and errors can be corrected simply by reloading from main memory. For fault-tolerant systems, PA-RISC processors also implement a feature that allows processors to run in lockstep with each other and detect execution discrepancies.

HP has also made some architectural enhancements to the 8700, adding features such as data prefetching, a quasi-least-recently-used (LRU) replacement policy for the data cache, and a 44-bit physical address space. This expanded 16-terabyte physical address space is useful for extremely

large data sets, which can utilize more than 1 terabyte of memory, the limit for previous 8x00 processors. The addition of prefetching capabilities accelerates some data transactions by fetching an additional cache line after a cache miss. Data prefetching and the quasi-LRU data cache will add some measure of architectural performance improvement, although probably not much.

Clearly HP is hedging its bets and protecting its customer base at the cost of two parallel development paths. The 8700 should keep its successful PA-RISC-based products competitive with other 64-bit servers until HP can migrate its customers to the IA-64 architecture. Ultimately, HP will offer IA-64 processors as a low-risk (no pun intended) path to greater performance beyond 2002. ♦

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