

PA-8500's 1.5M Cache Aids Performance

But HP Chip Is Likely to Trail 21264 When It Ships in 2H98



by Linley Gwennap

HP revealed a few more details of the PA-8500 at last month's Microprocessor Forum. The company is still being cagey, however, since the device has not taped out and system shipments are not expected until 2H98. The processor's unique design, which includes a stunning 1.5M of on-chip primary cache, appears likely to fall behind Digital's 21264 in both schedule and SPEC95 performance, but the HP chip may come out ahead when running applications that take advantage of the large cache.

Fast SRAM With Integrated CPU

As Figure 1 shows, the cache is divided into a 512K instruction cache and two 512K banks of data cache. The caches are four-way set associative, providing a better hit rate than an external direct-mapped cache of the same size. In fact, on some applications, these caches will have hit rates similar to the direct-mapped 2M caches typically used by HP systems today. The data-cache tags are stored in duplicate arrays, allowing snoop transactions to proceed in parallel with cache accesses.

The new chip uses essentially the same CPU core as the current PA-8200, which is built in a 0.5-micron process. Due

to the shrink to 0.25-micron CMOS, that core (excluding the bus interface) now occupies only 26% of the die. At the Forum, PA-8500 designer Bill Queen said his chip will reach at least 360 MHz, about 50% faster than the PA-8200. Due to the magnitude of the process change, we would not be surprised to see the PA-8500 reach 400 MHz or more.

The new core has a few improvements over the PA-8200 (see MPR 10/28/96, p. 18), mainly in the area of branch prediction. The size of the branch history table (BHT) is increased to 2,048 entries, twice the size of the PA-8200's rather meager BHT. The new BHT uses "agrees" mode (see MPR 11/17/97, p. 22) to improve the prediction accuracy when multiple branches map to the same entry in the BHT. Finally, the size of the TLB is increased by 33% to 160 entries, improving performance on applications, such as transaction processing, that make heavy use of the TLB.

To feed the faster core, HP has doubled the bandwidth of its Runway bus, which it has used in its high-end processors since the PA-7200 (see MPR 3/7/94, p. 12). The new interface transfers data on both edges of a 120-MHz clock, producing a peak bandwidth of nearly 2.0 Gbytes/s. Because the Runway bus is multiplexed, however, the best sustainable bandwidth is just over 1.5 Gbytes/s. Maintaining a 240-MHz data rate will be tricky, but HP has plenty of experience with high-speed system design.

Integrated Cache Provides Cost Savings

The PA-8500 will set a record by including 130 million transistors, more than 95% of them in the large caches. HP did not disclose the chip's die size, but Queen admitted it is "a bit larger" than current PA-8x00 chips, which measure a hefty 345 mm². The large cache arrays, however, incorporate redundant elements, so they are not susceptible to most defects. As a result, the yield will be at least twice that of the PA-8200. Eliminating the off-chip cache buses reduces the pin count from 1,081 to a more manageable 550. As a result, the PA-8500 will cost about \$160 to manufacture, according to the MDR Cost Model, compared with \$260 for the PA-8200.

The cost savings don't stop there. The on-chip caches eliminate the expensive external caches used by the PA-8200, slashing another few hundred dollars from the system cost.

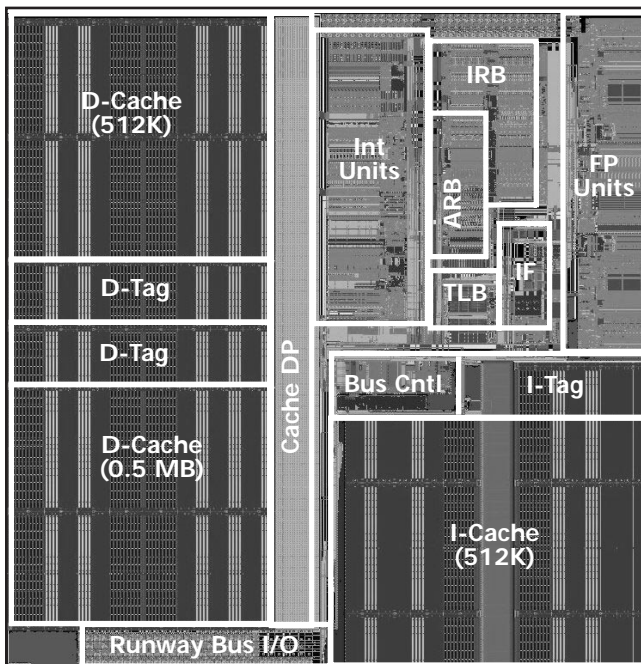


Figure 1. This die plot shows the PA-8500, which will be built in a 0.25-micron four-layer-metal CMOS process using C4 die attach, which eliminates the pad ring. HP did not reveal the die size.

For More Information

HP does not sell its PA-RISC processors on the open market. For more information on these processors, try www.hp.com/computing/framed/technology/micropro.

The PA-8200 uses a complex PC board to route the high-speed cache signals; the new chip is much easier to put on the system board. Thus, the PA-8500 will materially reduce system cost while providing a large performance boost.

Power dissipation will also improve. Queen would not disclose the PA-8500's power consumption but said it is cooler than the current parts, mainly due to a big drop in supply voltage from 3.3 V to 1.8 V. Eliminating the external cache provides further system-level power savings.

HP has not yet revealed the fab for the PA-8500, but since the company has no 0.35-micron capacity, much less the 0.25-micron process needed for the new chip, it is likely to use an outside source. Given its partnership with Intel, that company is a logical choice, but HP might also turn to AMD or to a foundry with leading-edge capacity.

Not Quite the Last PA-RISC Chip

Over the past summer, HP began dropping hints that it would deploy another PA-RISC processor after the PA-8500, and HP's Queen revealed that chip will be called the PA-8700. Although he declined to provide any details about the device,



HP project manager Bill Queen explains the benefits of the large primary caches on the PA-8500.

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we suspect it is simply a 0.18-micron shrink of the PA-8500, since most of HP's designers will soon be working on IA-64 chips. The PA-8700 probably won't appear before 2H99, so it is likely to ship after Merced and offer lower performance. Thus, the RISC chip offers HP an insurance policy in case Merced is late or slow, and it offers a crutch to PA-RISC customers who don't want to transition to IA-64 immediately.

In fact, the aging PA-8x00 core appears likely to fall behind Alpha in the performance race as early as next year, despite the PA-8200's current position as the industry's fastest processor. HP says the PA-8500 will deliver 30 SPECint95 and 50 SPECfp95 (base), but given the performance of the

236-MHz PA-8200, clock speeds of 400 MHz or more may be needed to reach these figures.

Given Digital's claim that the 21264 will deliver more than 40 SPECint95 and 60 SPECfp95 (base), HP has backed away from earlier statements that the PA-8500 will deliver industry-leading performance. Queen expects the PA-8500, with its large primary caches, will deliver better performance than the Alpha chip on at least some applications. To prove its point, however, HP must deliver its processor. 