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IBM Raises Curtain on Power5

More Details Disclosed at Microprocessor Forum

By Peter N. Glaskowsky {10/14/03-01}

IBM provided further insight into the evolution of its Power processors with a detailed presentation on Power5 at **Microprocessor Forum 2003**. Power5 will take over as the flagship of IBM's server processor family, adding multithreading and increased integration to the basic design of IBM's Power4. Power5 offers impressive scalability: IBM described servers based on Power5 as having up to 64 processors, 1,152M of L3 cache, and a terabyte of physical RAM.

The MPF03 talk built on the information offered at Hot Chips 2003, which focused on the multithreading features of the new processor. (See *MPR 9/8/03-02*, "IBM Previews Power5.") At MPF, IBM showed how the Power5 pipeline differs from that in Power4. Figure 1 shows how the key elements in the Power5 core are connected and how some elements are duplicated to support multithreading.

Chip and System Designs Also Enhanced

Other significant changes from Power4 to Power5 are reflected in the new chip's increased level of integration. The Power5 brings memory control onto the die and relocates the

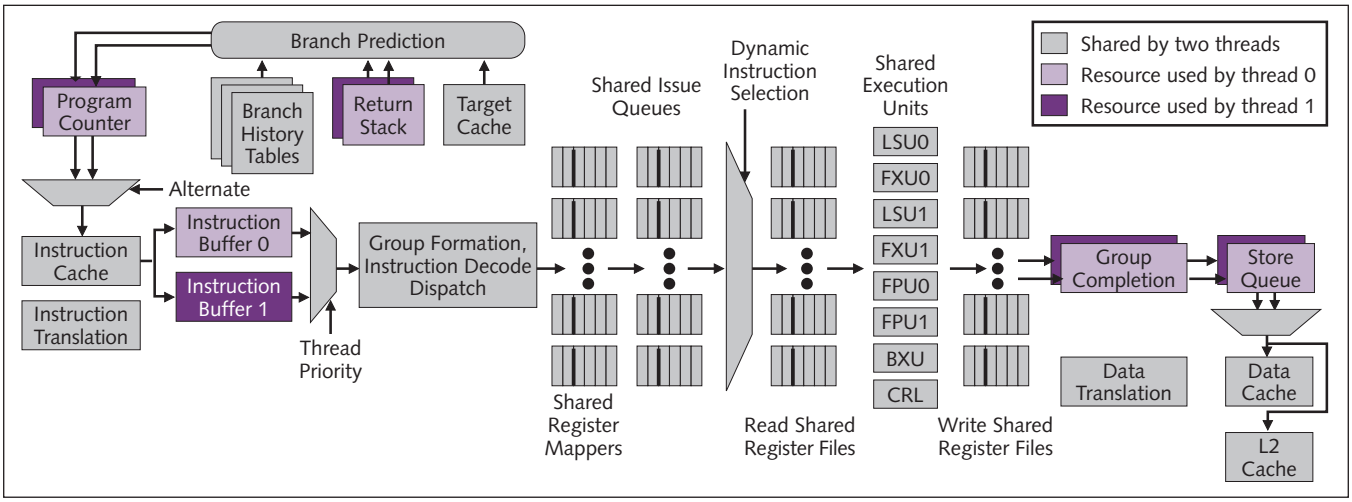

Figure 1. The Power5 pipeline includes duplicated program counters, instruction buffers, and branch-predictor return stacks to support multithreading. In other respects, the new design is similar to that of the Power4.

Price & Availability

IBM's Power5 processor will be available in systems in 2004. The Power5 chip will not be sold separately.

L3 cache interface, coupling both subsystems more closely to the CPU. As Figure 2 shows, the Power5 design connects the off-chip L3 cache—a 36M embedded-DRAM device—to the on-chip L2 cache. The Power5 L3 has a 12-way set-associative design and has a smaller line size (256B vs. 512B) than its predecessor has. The smaller line size doubled the number of directory entries in the Power5's on-chip L3 controller.

Power5's L2 cache is somewhat larger—1.92M vs. 1.44M in the Power4—and is 10-way set-associative, up from the 8-way design of the Power4 L2. The L1 caches in the Power5 are the same size as those in the Power4: 64K for instructions, 32K for data.

As before, the Power5 is intended for assembly into a multichip module, combining four processor chips and four L3 cache RAMs. The Power5 module, which includes eight physical processor cores and operates as a 16-way node by virtue of the new core's multithreading features, is only 95mm × 95mm in size (slightly smaller than the Power4 module) and has 4,491 I/O signals. Power5 systems can address up to one terabyte of physical memory, twice the addressing range of the Power4.

The Power5 die includes an enhanced version of the distributed switch interface found on Power4. Interfaces used to communicate between processors on the Power5 module run at the full core speed of the chip; off-module interfaces run at half this rate. At MPF, IBM showed system configurations using two and eight modules with 16 and 64 physical processors (32 and 128 virtual processors), respectively.

IBM has used its 130nm process for Power5. This process uses silicon-on-insulator (SOI) technology and eight

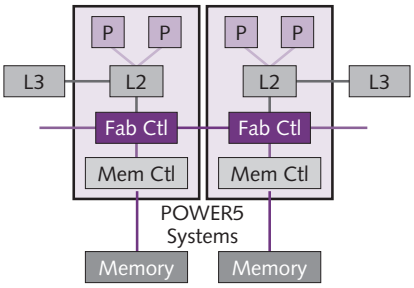

Figure 2. Power5 includes an integrated memory controller, previously an off-chip component in Power4 systems, and locates the L3 cache controller closer to the L2 cache to reduce access latencies.

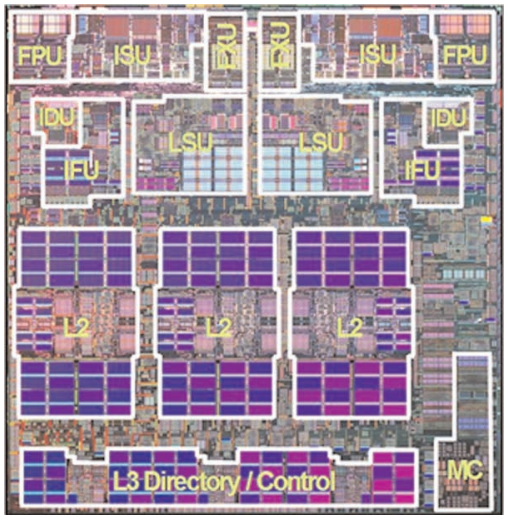

Figure 3. The Power5 die is structured much like the die of the Power4. The greatest differences are shown in the area of the L2 caches and the L3 cache controllers. The new memory controller is also shown here.

layers of copper interconnect. The chip is 389mm^2 in size, contains 276 million transistors, and has 2,313 signal and 3,057 power connections. The 130nm Power4+ processor, by comparison, has 184 million transistors and a die area of 267mm^2. Apart from the increased integration, IBM attributes much of the growth in transistor count to multithreading, which added about 24% to the size of each core. The company did not reveal a clock-frequency target for the Power5, nor did it reveal power-consumption figures. Figure 3 shows a labeled photo of the Power5 die.

Roadmap Extended

The Power5 is running now in IBM's labs and will arrive in commercial systems during 2004. IBM also updated its Power roadmap at MPF03, showing a 90nm Power5+ shipping in systems in 2005 and a 65nm Power6 processor with "advanced system features" shipping in 2006.

We expect IBM to use the 90nm process for a Power4 derivative—a version of the PowerPC 970 used in Apple's G5 systems—for 2004 shipments. Such a product would help IBM prove out the 90nm process before committing to it for server systems. We also expect IBM to produce a Power5 derivative for Apple in late 2004, but there is no indication of whether this chip would be made in the 130nm or the 90nm process.

Now that IBM has a volume customer for Power-series cores, it may be able to accelerate the pace of development for these chips. IBM faces increasingly strong competition from Intel and Sun and must move quickly to maintain its market share.